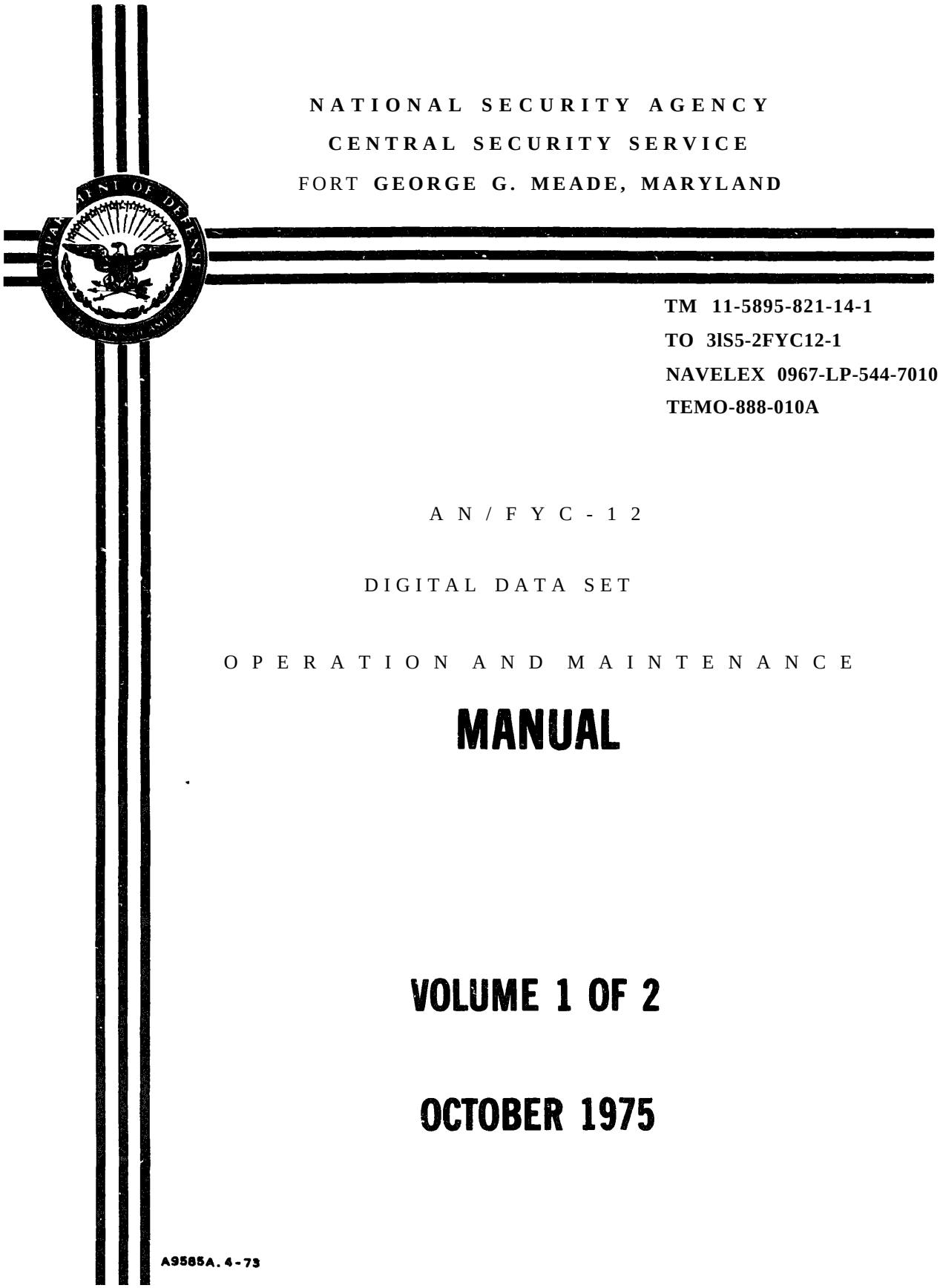

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AN/FYC-12

DIGITAL DATA SET

OPERATION AND MAINTENANCE

MANUAL

VOLUME 1 OF 2

OCTOBER 1975

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INTRODUCTION

This manual provides installation, operation and maintenance instructions for the Digital Data Set AN/FYC-12. In addition, it contains principles of operation and illustrated parts breakdown chapters as supplementary technical information for maintenance purposes. This manual is divided into two volumes.

Volume I contains the following:

Chapter 1	Description of Equipment
Chapter 2	Installation
Chapter 3	Operating Instructions
Chapter 4	Principles of Operation
Chapter 5	Preventive Maintenance
Chapter 6	Corrective Maintenance

Volume II contains the following:

Chapter 7	Illustrated Parts Breakdown
Appendix	(Maintenance Illustrations)

The Digital Data Set AN/FYC-12 Technical Manual has been written for cryptologic technicians whose technical education competence shall equal that of a graduate of a military service school course in electronics of no less than 40 weeks duration.

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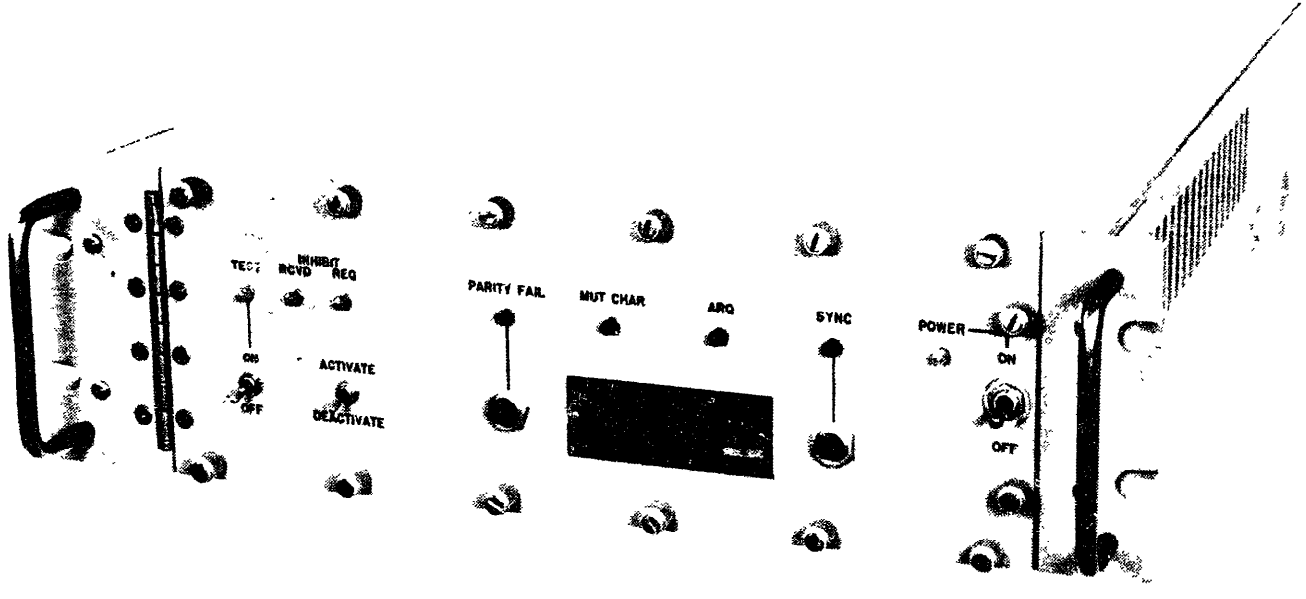

Figure 1-1. Digital Data Set AN/FYC-12

CHAPTER 1

DESCRIPTION OF EQUIPMENT

I - CLASSIFICATION OF EQUIPMENT

1-1. CLASSIFICATION OF EQUIPMENT. -The Digital Data Set AN/FYC-12 and this manual are unclassified.

II - GENERAL DESCRIPTION

1-2. PURPOSE OF EQUIPMENT. - This manual covers the operation and maintenance of the Digital Data Set AN/FYC-12, illustrated in Figure l-l. The equipment is used to detect and correct transmission errors in digital communications systems.

1-3. FUNCTIONAL DESCRIPTION. - The Digital Data Set AN/FYC-12 functions as part of the Digital Data Telecommunications System. It operates in full duplex communication loops using start-s top or bit stream (continuous data) terminal equipment at transmission rates between 75 and 9600 baud. The AN/FYC-12, which is completely code transparent in all modes of operation, must have control of the data source with a clock step-character (start-stop) or clock step/bit (bit stream). The output code to the data sink is identical to the input code from the data source. The terminal codes from the data source are encoded into constant ratio codes for transmission to a distant receiver, and stored in a cyclic TTL (Transistor -Transistor Logic) memory of adjustable length (maximum 64 characters). The input terminal code, not the constant ratio code, is stored. The distant receiver is able to distinguish non-constant ratio codes or unused codes from received communication (errors) and automatically request retransmission from the local transmission memory. This function is known as ARQ (Automatic Retransmission Request) . The operator may resynchronize the system automatically or close down the distant transmitter (Inhibit Activate) by using **super**-visory characters . A typical system configuration (Figure 1-2) indicates that each Digital Data Set AN/FYC-12 consists of transmitter and receiver sections at the local and distant locations.

a. System Operation. - The local (AN/FYC-12) transmitter obtains data upon request from the local Digital Data Terminal (Teletype), stores it in a cyclic memory and encodes it into a constant ratio code before transmitting the data to the distant receiver. The distant (AN/FYC-12) receiver checks the incoming data and, if valid (constant ratio used code), decodes the con - stant ratio code to the original terminal code and outputs it to a distant data terminal (Teletype). The distant transmitter sends data from distant to local data terminals in the same manner. If invalid data (non-constant ratio or

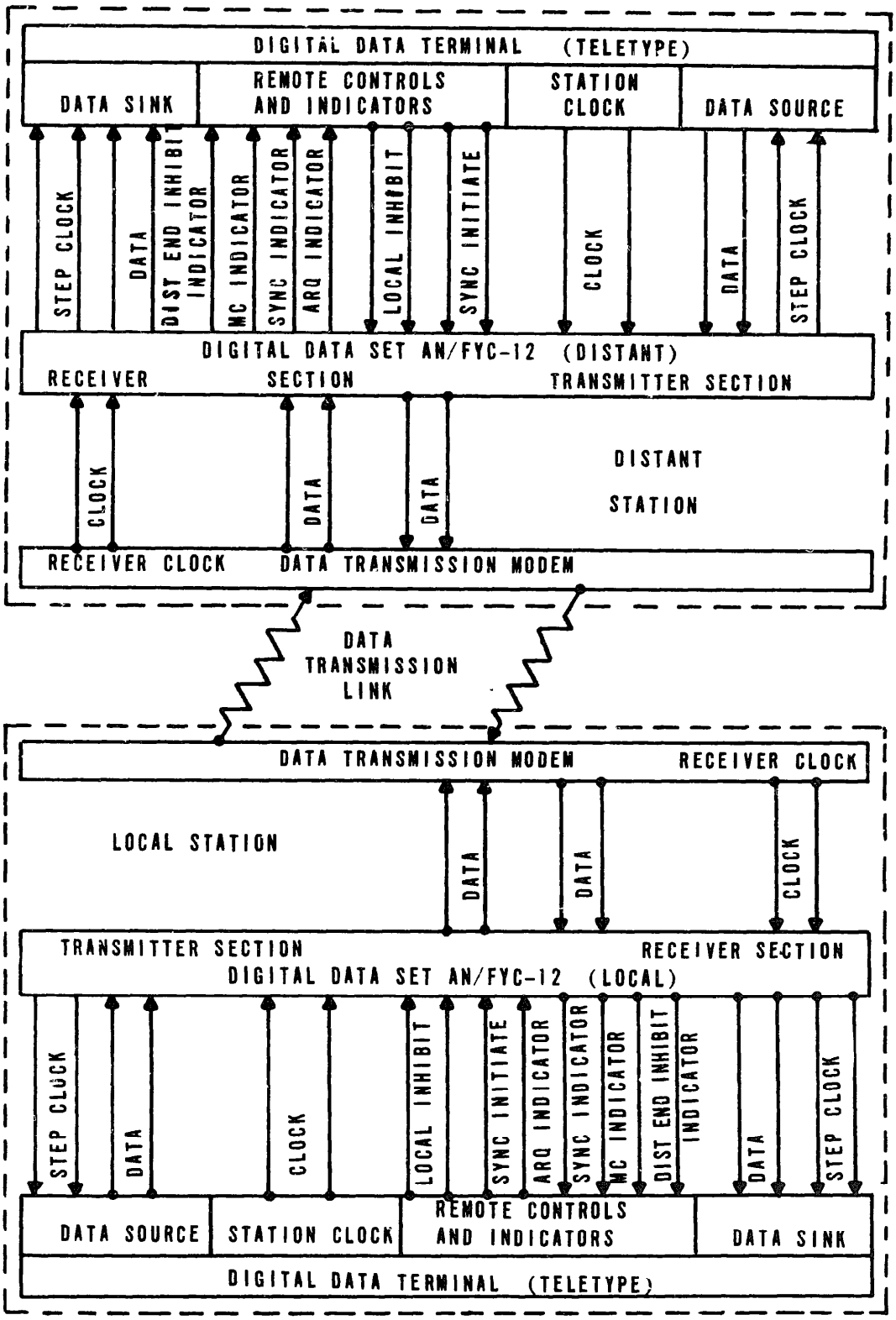

Figure 1-2. System Configuration

unused code) is received, the receiver requests retransmission (ARQ) by raising a flag to the distant transmitter. The transmitter completes the active character, inhibits the distant data terminal for one memory cycle, then writes and transmits two ARQ supervisory characters followed by the contents of the transmitter memory. After a transmission &lay the local receiver detects the ARQ supervisory characters and raises a flag to the local transmitter, which completes the active character, inhibits the local data terminal, and enters the ARQ cycle. Thus, the local and distant data terminals are closed down and both transmitters are sending from memory. The distant receiver receives the character that caused error as the first character after the distant source terminal inhibit has been removed, and rechecks it for validity. If a valid character is sent to the distant data terminal, both ends of the communication link leave the ARQ cycle. The request for ARQ can be from either receiver, so that data errors in each direction can be detected and corrected. No data is lost, added, or invali-&ted, but communications are closed down for one memory cycle so that extra time is required to complete transmission. If constant invalid data is received at either end, the system continues to repeat the ARQ cycle, closing down communications. (This results from a hardware fault or loss of synchronization between transmitter and receiver.) The operator may initiate "Sync Cycle" , which re-synchronizes the system and probably alleviates the repeating ARQ cycle. If the synchronization has not moved by more than four bits backward or forward, no data will be lost, added, or invalidated from transmitted communication after repeated ARQ cycles and re-synchronization. The operator can control the distant transmitter with two supervisory characters . "Inhibit Activate" closes down or lights the "Inhibit Request" indicator (strap option) and "Inhibit Deactivate" opens data communications. See paragraph 4-4 for complete details of "ARQ Cycle", "Sync Cycle", "Inhibit Activate" and "Inhibit Deactivate. "

b. Summary of Capabilities. - A summary of technical characteristics of Digital Data Set AN/FYC-12 appears in paragraph 1-7.

1-4. PHYSICAL DESCRIPTION. - The Digital Data Set AN/FYC-12 consists of one unit. Physical dimensions are given in Table **1-1** Equipment Supplied.

Table 1-1. Equipment Supplied

QUAN.	FIG. REF.	ITEM	DIMENSIONS (inches) W	H	D	WEIGHT (lbs) (uncrated)
1	1-1	AN/FYC-12	19	5 1/4	24*	56

*(overall depth including handles, 26)

The Digital Data Set AN/FYC-12 may be broken into two major assemblies: Al Steel cabinet and A2 Electronic chassis and card file.

a. Steel Cabinet Assembly Al. - The cabinet assembly is designed to minimize radio frequency interference and is equipped with eight knock-out holes 1-3/8 inches diameter in different positions for ease of interconnection cables which should run in a steel conduit. The battery power supply ±6V DC is connected to terminal board T-l located on this assembly.

b. Electronic Chassis Assembly A2. - This sheet metal chassis with a hinged front panel is designed to compactly package (a) electronic circuit cards, (b) front panel indicators and controls, (c) set-up and initialize controls, and (d) DC-DC converter power supply. Figure 1-3 illustrates the chassis assembly removed from cabinet. The component assemblies of the chassis assembly are detailed in paragraph 1-7. Electronic circuit card assemblies A2A1 through A2A11 are designed to plug into a card file and can be removed easily, using the card extractor supplied with the unit. They are numbered consecutively from left to right. Assemblies A2A12, A2A13 and A2A14 are hard wired together by cable harness and are considered not removable from the electronic chassis assembly. The DC-DC converter (power supply) A2A17 is a completely sealed and non-repairable assembly. It can be readily removed by disconnecting connectors P1 and P2 and the mounting hardware. The converter package then slides out of the A2 chassis assembly easily. A rear view of Digital Data Set AN/FYC-12 with rear cover removed is shown in Figure 1-4. The interconnection terminal boards T-l (battery power supply), TB-3, TB-4, and TB-5 (line signals) are clearly illustrated.

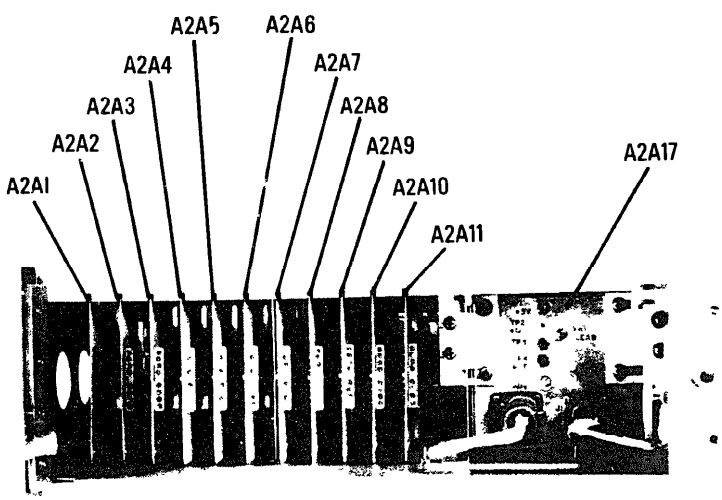

Figure 1-3. Chassis Assembly
(Removed From Cabinet)

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SIGNAL TERMINAL BOARDS

DC INPUT TERMINAL BOARD A1TB1

A2TB5

A2TB4

A2TB3

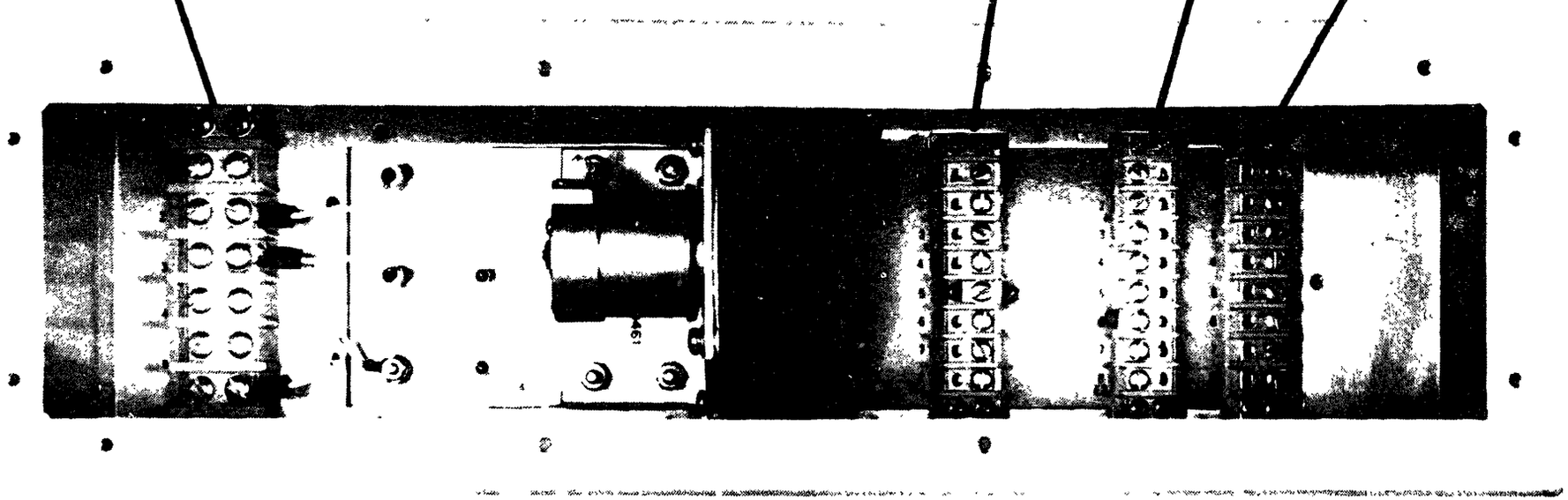


Figure 1-4. Digital Data Set AN/FYC-12 (Rear View)

1-5. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - The following equipment is necessary but not supplied, to connect Digital Data Set AN/FYC-12 into the system:

Table **1-2.** Equipment Required But Not Supplied

QUANTITY	ITEM
	Steel conduit **1-3/8** inches diameter
	Interconnecting cable (power and signal)
	Electrician's Tool Kit

For maintenance or troubleshooting the AN/FYC-12, the following **equip**ment is required:

1. Extender card assembly (ON199640)
2. Integrated circuit test clip for 14 pin and 16 pin IC's
3. High quality oscilloscope, Tektronix 545B (or equivalent)
4. High quality test meter, Simpson 260 (or equivalent)
5. Digital pulse counter, H. P. 5245L (or equivalent)

III - QUICK REFERENCE DATA

1-6. EQUIPMENT IDENTIFICATION. - Digital Data Set AN/FYC-12.

1-7. ELECTRICAL CHARACTERISTICS. - Electrical characteris tics of the Digital Data Set AN/FYC-12 are as follows:

5. DC Input Power Required.

Voltage	+6 **Volts ±1V** and -6 Volts ±1V or 12 Volts ±2v
Current	6 Amps
Dissipation	72 Watts

b. Line Signals. - All line signals must meet MIL STD 188C for low level digital interface signals.

c. Input Signals. - Serial input data is at modulation rates between 75 and 9600 baud. An external system provides the station clock at two times the data rate. Remote control inputs for "Synchronization" and "Inhibit Activate" are +6V levels.

d. Output Signals. - Transmitter output is continuous data at modulation rates between 75 and 9600 baud, Data to local terminal (sink) are identical to input data from terminal (source). Local terminal (source) clock step is +6V for one bit time (bit stream) and two bit times (start-stop). Local terminal (sink) clock step is six cycles of receiver clock (bit stream) or +6V for one bit time (start-stop). The system provides four status or alarm conditions that are activated by +6V. They are:

1. Mutilated Character
2. ARQ Cycle
3. Sync Cycle
4. Distant End Inhibit

Table 1-3 tabulates additional electrical characteristics of the system, A list of the Electronic Chassis Assemblies is given in Table 1-4.

Table 1-3. Characteristics of the AN/FYC-12

SYSTEM	
Data Rate -	75-9600 Baud (MIL STD 188C)
Station Clock -	Twice Data Rate
Synchronization -	Automatic After Manual Initiation
Number Channels -	Single Channel Full Duplex
Line Interface -	DC Low Level (MIL STD 188C)
TRANSMITTER	
Input Data	Serial data in any of the following input formats (MIL STD 188C): 1 - Bit Stream 2 - 5-Bit Start-Stop 3 - 6-Bit Start-Stop

Table 1-3 (Continued)

	4. 7-Bit Start-Stop 5. 8-Bit Start-Stop
Output Data -	Serial data constant ratio codes output formats (MIL STD 188C): 1. Bit Stream and 5 Bit Start-Stop input formats transmitted in eight bit constant ratio code 2. 6,7-and 8-Bit Start-Stop input formats transmitted in 11 bit con - stant ratio code
Source Step Clock -	Step clock to data source in phase with the station clock. Low level DC inter - face (MIL STD 188C) 1. Bit Stream input format has six periods (one bit accepted/period) of station clock for each output character. 2. Start-Stop input formats have high level (+6V) for two periods of station clock for each output char - acter.
Memory -	Solid state TTL memory adjustable in length between eight and 64 characters in four character steps. Parity bit added to memory to detect memory errors.
Input Bit Timing -	The data source is enabled by the source step clock, but the first data bit may be delayed as much as two bit times. In Start-Stop input modes, the start bit (always low) is used to measure the delay and, hence, center sample remainder of the character. If no start bit is detected during the first two bit times, the “Idle Supervisor”

Table 1-3 (Continued)

is transmitted. In the Bit Stream input mode there is no start bit, and &lay must be measured and the center sample switch adjusted with an oscilloscope before transmission can begin.

Cons tan t Ratio Codes -

The terminal data codes are encoded by the transmitter into "Constant Ratio Codes" (all characters have four l's). This type of code has redundancy and requires more data bits than the terminal data codes, but allows errors to be detected at the distant receiver. Two lengths of constant ratio codes are used:

1. Bit Stream
   5-Bit Start-Stop } 8 Bits/Character

2. 6-Bit Start-Stop
   7-Bit Start-Stop
   8-Bit Start-Stop } 11 Bits/Character

Supervisory Characters -

In addition to normal data transmission between the transmitter and the distant receiver, the transmitter can control the distant AN/FYC-12 with six supervisory characters that are used to control the communication system. The six supervisory characters are:

1. Idle
2. Inhibit Activate
3. Inhibit Deactivate
4. ARQ Request
5. Sync A
6. Sync B

Table 1-3 (Continued)

ARQ Cycle -	If the receiver has detected an error, it automatically requests a retransmission (ARQ). The transmitter adds two "ARQ" supervisory characters the memory and then repeat the contents of its memory. This results in both ends of the data link retransmitting from memory (ARQ) and is called "ARQ Cycle. "
sync Cycle-	The receiver must be synchronized to the transmitter for data communication. A unique bit sequence, "Sync A" supervisory character followed by "Sync B" supervisory character, generates eight l's, which are used by the receiver to obtain correct synchronization. After "Sync A" and "Sync B" are transmitted, supervisory characters "Inhibit Activate" or "Inhibit Deactivate" are used to check that correct synchronization has been achieved. Note that supervisory characters used during "Sync Cycle" are not stored in the memory.
Inhibit Activate -	The distant transmitter may be closed down or requested to close down- (strap option) with the "Inhibit Activate" supervisory character, and reopen data communications with the "In hibit Deactivate" supervisory character. Note that the distanttransmitter is always sending valid constant ratio line codes. When inhibited, it repeatedly sends an "Inhibit Deactivate" supervisory character or "Inhibit Activate" supervisory character, depending upon the position of the Inhibit Switch.

Table 1-3 (Continued)

Strap Option -	The transmitter inhibit control logic may operate in two ways, depending upon the “strap option” (reversible plug located on assembly A2A4).
It may -	1. Automatically close down when an Inhibit Activate supervisory character is received from the distant end. 2. Light the “Inhibit Request” indicator on the front panel when an “Inhibit Activate” is received.

RECEIVER

Input Data -	Serial data/constant ratio codes. DC Low Level Interface (MIL STD 188C) in two formats: 1. 8-bit Constant Ratio (four l’s) 2. 11-bit Constant Ratio (four l’s)
Receiver Clock -	External receiver clock at twice the data rate. The fall of the receiver clock is at the center of each received bit.
Output Data -	Serial data in any of the following switched formats (Start-Stop formats have start and stop bits added). Code: are identical to those accepted by the transmitter. 1. Bit Stream 2. 5-Bit Start-Stop 3. 6-Bit Start-Stop 4. 7-Bit Start-Stop 5. 8-Bit Start-Stop

Table 1-3 (Continued)

Sink Step Clock -	Step clock to data sink in phase with the receiver clock. Low level DC interface (MIL STD 188C). 1. Bit Stream format has six periods of step clock per correct character received. 2. Start-Stop input formats have high level (+6V) for one period of receiver clock for each correct character received.
Mutilated Character -	If the receiver detects a character that does not have four 1's (not con - stant ratio code) or is unused in selected input format, the receiver declares the character mutilated in transmission, closes the data sink for one memory cycle, and requests retransmission ARQ.
Idle Supervisor -	The receiver outputs to the data sink a character that consists of all l's (no start bit) and the normal step clock (used only in Start-S top modes).
Test Mode -	In the test mode of operation the local transmitter is connected directly to the input of the local receiver. The transmitter and receiver clocks are also made common. CAUTION. - When the AN/FYC-12 is placed in test mode an "ARQ Cycle" is forced, and input data is lost from future transmission. The test mode is useful for single end setup and fault finding.

Table 1-4. Electronic Chassis Assembly

A2A1	DATA SAMPLE GEN ASSY
A2A2	FAST CLK STEP GEN ASSY
A2A3	IN CONT XFR CLK GEN ASSY
A2A4	XMTR SYNC AND ARQ CONT ASSY
A2A5	CONST R CODE GEN ASSY
A2A6	DATA INP COD RAM CNTR ASSY
A2A7	RECRC MEMORY ASSY
A2A8	LEVEL CONVERTER ASSY
A2A9	RCVR DATA PROCESSOR ASSY
A2A10	RCVR CONT LOGIC ASSY
A2A11	RCVR ARQ AND SYNC CONT ASSY
A2A12	FRONT PANEL ASSY
A2A13	BACK PLANE ASSY
A2A14	INTERFACE ASSY
A2A15	TOP FRAME ASSY
A2A16	CHASSIS ASSY
A2A17	DC-DC CONVERTER ASSY

1-8. ENVIRONMENT. - Optimum ambient environmental conditions for the Digital Data Set are as follows:

1. Operating temperature	0°C to +50°c
2. Non-operating temperature	-15°C to +75”C
3. Heat dissipation	72 Watts
4. Humidity	Up to 95% with condensation

CHAPTER 2

INSTALLATION

I - UNPACKING AND INSPECTION

2-1. PACKAGING DATA. - The unpackaged weight of the Digital Data Set AN/FYC-12 is 56 pounds; the packaged weight is approximately 80 pounds. The crated unit measures 25 inches wide x 32 inches deep x 16 inches high.

2-2. UNPACKING. - The Digital Data Set AN/FYC-12 is packed in a container prepared for overseas shipment in accordance with Level A of specification MIL-E-17555G and Level C for domestic shipment. Upon receipt of the unit, carefully unpack the unit near the area where the unit is to be installed. The area should be large enough to allow removal from the carton. No special equipment is required for unpacking. Unpack the unit according to the following procedure:

1. Cut the banding straps on the outer container.
2. Open the outer carton and remove the cushioning on top and sides.
3. Cut the barrier bag at the heat seal in the overseas package and remove the inner container.
4. Open the inner carton and remove the desiccant bags and the cushioning from the top and sides of the unit.
5. Remove the manual and the Digital Data Set AN/FYC-12.
6. Remove the protective sleeve from the front of the AN/FYC-12.

The shipping containers and packing materials may be retained for reshipment.

2-3. INSPECTION PROCEDURE. - When the AN/FYC-12 is free of the shipping container, inspect it for dents, cracks, and security of access panels. Inspect the front panel for broken indicators or switches. When inspection of the external surfaces is complete, unfasten the captive screws (14) on the front panel assembly and open the panel. Check the eleven circuit cards (A2A1 through A2A11) to be sure each is inserted in its respective connector. Check the DC-to-DC converter assembly A2A17 to be sure it is securely fastened in the unit, and that connectors P-l and P-2 are tightly secured. After inspection is complete, close the front panel and secure the captive screws.

2-4. DAMAGE REPORT. - It is important to report any damage discovered during the inspection outlined in paragraph 2-3. Follow the instructions issued by the custodial department or agency.

II - INSTALLATION PROCEDURE

2-5. GENERAL. - The Digital Data Set AN/FYC-12 is designed for installation in an RR-197 relay rack, or equivalent. It has four slotted holes through the front panel for mounting hardware and has eight 1-3/8 inch diameter knockouts, two each in the sides, top and bottom of the unit. Interconnections can be made through any of the openings. It is recommended that the power connections be made through a knock-out at the right side when viewing the unit from the front, and tie signal connections through a knock-out on the left side of the unit. These openings are designed to accept connectors for a 3/4 inch thin wall conduit. An outline drawing of the Digital Data Set AN/FYC-12 is shown in Figure 2-1.

2-6. TOOLS AND TEST EQUIPMENT. - No special tools or test equipment are required during the installation and alignment of the equipment.

2-7. LOCATING THE EQUIPMENT. - The Digital Data Set AN/FYC-12 should be located in an open slot of the RR-197 relay rack that has a minimum of 5-1/4 inch vertical clearance. The operating and non -operating environmental limitations are listed in paragraph 1-8. Access to the rear panel is necessary during installation. During normal operation access to the front panel only is required; however, in order to adequately ventilate the unit, the area to the rear and right sides should be clear of obstructions.

2-8. EQUIPMENT MOUNTING. - Before installing the equipment, remove the rear cover. Punch out as many knock-outs as needed for cable entry. Select a knock-out on the right. top, bottom, or side of the unit (when viewed from the front) for the DC power cable and one on the left top, bottom, or side of tie unit for the signal cables. Place the AN/FYC-12 in the rack and install four 10-32 screws 1/2 inches long through the slotted holes in the front panel. After the unit is attached to the rack, the conduit for the interconnection wires should be installed. The power and signal cables should be physically separated as much as possible. Figure 1-4 is a rear view of the AN/FYC-12 showing the input and signal terminal board locations.

2-9. CABLE FABRICATION. - Install the power cable in a cable entry tube and pull the cable through the rear access panel so that the input power terminations can be cut to size and the power cable fabricated outside the unit. A minimum of No. 14 gage insulated copper wire should be used for the input. power connections. After the harness has been fabricated, pull the input cable back through the cable entry tube, secure the cable, and connect the input connections in accordance with Table 2-1.

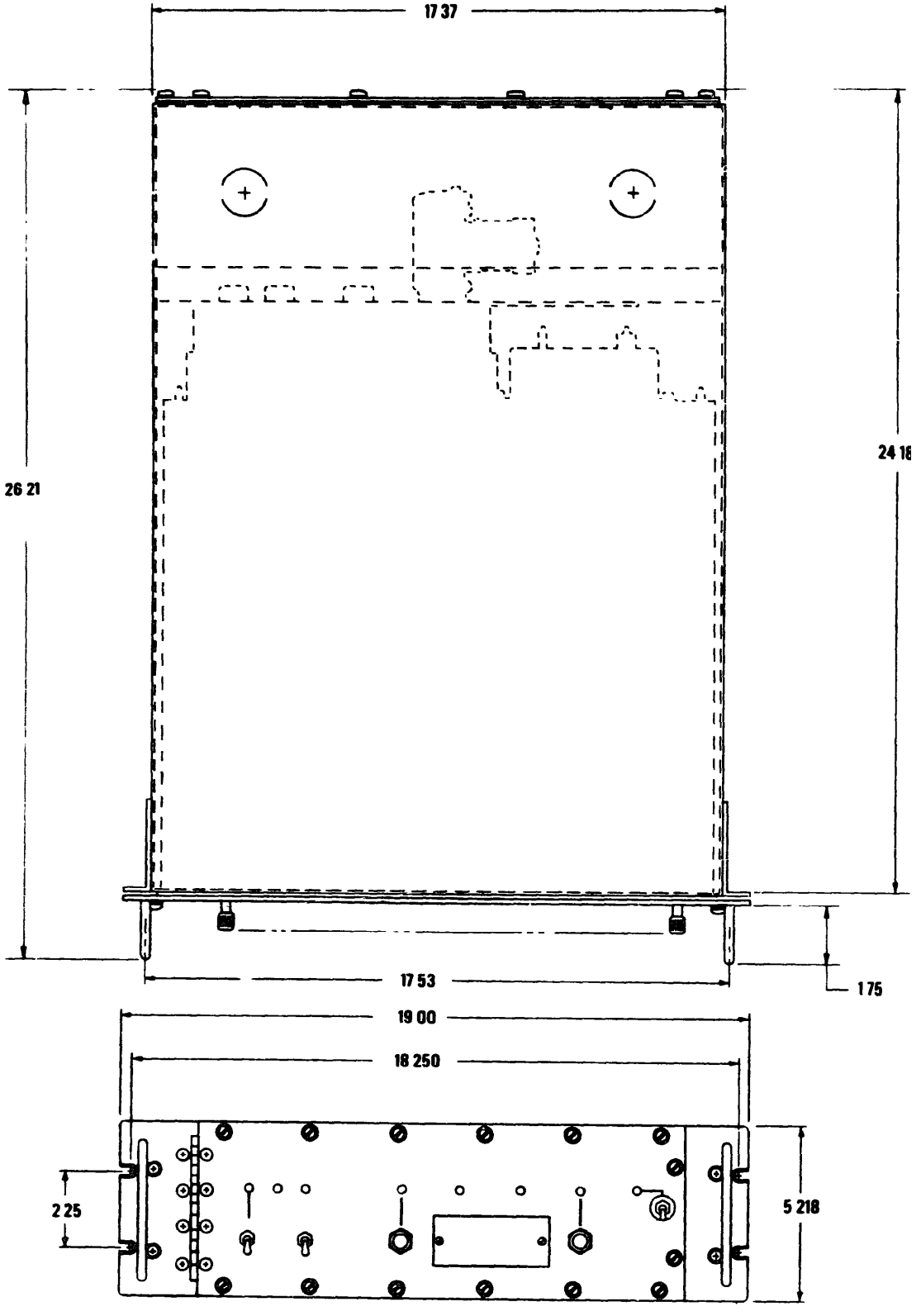


Figure 2-1. Digital Data Set AN/FYC-12 Outline Drawing

Table 2-1. Power Interconnections

Power Interconnection Cable to Terminal Board TB1 Located on Assembly A1. See Figure 1-4.			
From	Function	Terminal Number	Terminal Type
Battery (Plus)	+6 Volt Input	TB1-1*	No. 8-32 Screw
Battery (Minus)	-6 Volt Input	TB1-2*	No. 8-32 Screw
Battery (Common)	6 Volt Return	TB1-6**	No. 8-32 Screw

Note: - Terminals 3, 4 and 5 on TBl are not used.

*When DC power is provided by a 12-volt power supply, strap the grounded, or common side of the power supply, TB1-1 or TB1-2 as the case may be, to the equipment common terminal, TB1-6.

**When DC power is provided by a positive and negative 6-volt power supply, connect the grounded, or common power supply terminal to the equipment common terminal, TB1-6.

a. Signal Cable, - Install the signal cable on the left side of the unit, and fabricate the cable outside the unit, The signal connections are made to terminal boards TB-3, TB-4 and TB-5 of A2. Use six twisted shielded pairs for the external inputs. The shields on the six twisted pairs should be connected together and a ground lead connected to a ground lug located under TB-3 mounting screw. Use eight twisted shielded pairs for the outputs to the external system. Terminal 4-6 is provided with a terminal solder lug. Remove the lug and solder the return wire of three of the twisted pairs to this lug. The shields of these three pairs should be connected together and a ground wire connected to a ground lug located under the TB-4 mounting screw. Terminal 5-4 is provided with two terminal lugs. Remove the lugs andsolder three of the returns of the twisted pairs to one lug and two of the returns to the other lug. Tie the shields of the five pairs together and connect a ground wire to the lug located under TB-5 mounting screw. After the signal harness has been fabricated, pull the signal cable through the entry tube, secure the cable, and connect the input and output signal connections in accordance with Table 2-2.

Table 2-2. Signal Interconnections

Two signal interconnection cables are required:

a) Input signals to terminal boards TB3 and TB4

b) Output signals to terminal boards TB4 and TB5

Terminal boards TB3, TB4 and TB5 are all located on Assembly A2. See Figure 1-4.

From	Function	Terminal Number	Terminal Type
Data Terminal (Source)	Input Data	TB3-1	No. 5-40 Screw
	Data Return	TB3-2	No. 5-40 Screw
Data Terminal (Station Clock)	Clock Return	TB3-3	No. 5-40 Screw
	Station Clock	TB3-4	No. 5-40 Screw
Communications Modem	Clock Return	TB3-5	NO. 5-40 Screw
	Receiver Clock	TB3-6	NO. 5-40 Screw
Communications Modem	Receiver Input Data Line	TB3-7	No. 5-40 Screw
	Data Return	TB3-8	No. 5-40 Screw
Input Cable	Shielding	TB3 Ground	No. 6 Ground Lug
Data Terminal (Control)	Local Inhibit Return	TB4-1	No. 5-40 Screw
	Local Inhibit	TB4-2	No. 5-40 Screw
Data Terminal (Control)	Sync Initiate	TB4-3	No. 5-40 Screw
	Sync Initiate Return	TB4-4	No. 5-40 Screw

Table 2-2 (Continued)

To	Function	Terminal Number	Terminal Type
Data Terminal (Control)	ARQ Indicator	TB4-5	No. 5-40 Screw
	Return	TB4-6	No. 5 Lug
Data Terminal (Control)	M. C. Indicator	TB4-7	No. 5-40 Screw
	Return	TB4-6	No. 5 Lug
Data Terminal (Control)	Sync Indicator	TB4-8	No. 5-40 Screw
	Return	TB4-6	No. 5 Lug
Output Cable	Shielding	TB4 Ground	No. 6 Ground Lug
Communications Modem	Send Line Data	TB5-1	No. 5-40 Screw
	Return	TB5-4	No. 5 Lug
Data Terminal (Source)	Source Step Clock	TB5-2	No. 5-40 Screw
	Return	TB5-4	No. 5 Lug
Data Terminal (Sink)	Output Data	TB5-3	No. 5-40 Screw
	Data Return	TB5-4	No. 5 Lug
Data Terminal (Sink)	Sink Step Clock	TB5-5	No. 5-40 Screw
	Return	TB5-4	No. 5 Lug

Table 2-2 (Continued)

To	Function	Terminal Number	Terminal Type
Data Terminal (Control)	Distant End Inhibit Indicator	TB5-6	No. 5-40 Screw
	Return	TB5 - 4	No. 5 Lug
Output Cable	Shielding	TB5 Ground	No. 6 Ground Lug

Note: - Terminals 7 and 8 on TB5 are not used.

b. Check For Correct Connections. - After the power and signal inputs have been connected, check to see that the power and signal cable conductors have been connected to the appropriate terminal points within the AN/FYC-12. Install the rear cover to complete the installation procedure.

III - ADJUSTMENTS

2-10. LINE DRIVER CAPACITOR SELECTION. - The transmitter line driver capacitors installed in the equipment at the factory are selected to match low level DC interface specifications (MIL STD 188C) at the highest data rate (9600 baud). If the equipment is to be operated at a lower data rate then the line driver capacitors C-9 through C-16 on Assembly A2A8 must be changed in accordance with Table 2-3 to match (MIL STD 188C). The effect of the capacitors is to reduce the rate of change on the low level DC interface in order to minimize cross -talk and interference. Figure 1-3 shows the replaceable modules of the AN/FYC-12. Loosen the captive screws and open the front panel. Using the card extractor remove card assembly A2A8 (level converter assembly). Figure 2-2 shows the layout of the components; the eight line driver capacitors are mounted between terminals in the center of the card. Unsolder the eight capacitors and replace with values selected from Table 2-3. Once the capacitors have been installed, inspect to ensure that correct values were selected and good solder joints were made. Dress the capacitors to be below the height of IC's on the card and replace the A2A8 assembly in the AN/FYC-12. The equipment is now set to operate at the new baud rate, and the low level DC interface conforms to MIL STD 188C.

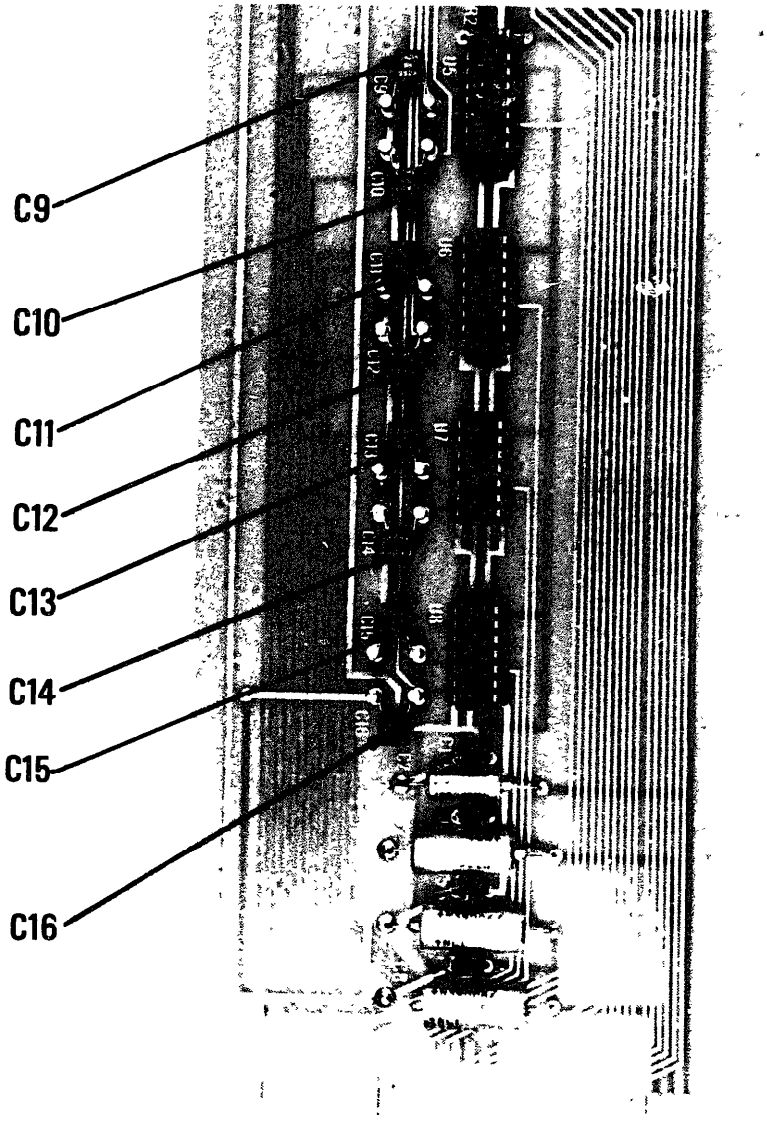


Figure 2-2. Level Converter Assembly A2A8

Table 2-3. Line Driver Capacitor Selection

Data Rate (Baud)	Capacitor Reference Numbers			
	C10, C11, C12, C13, C14, C15		C9 and C16	
	Value Micro-Farads	MIL Designation	Value Micro-Farads	MIL Designation
75	0.82	CK06BX824K	0.39	CK06BX394K
150	0.39	CK06BX394K	0.22	CK06BX224K
300	0.22	CK06BX224K	0.10	CK05BX104K
600	0.10	CK05BX104K	0.047	CK05BX473K
1200	0.047	CK05BX473K	0.022	CK05BX223K
2400	0.022	CK05BX223K	0.010	CK05BX103K
4800	0.010	CK05BX103K	0.0056	CK05BX562K
9600	0.0056	CK05BX562K	0.0033	CK05BX332K

Note: - The AN/FYC-12 is equipped with capacitors to operate correctly at 9600 baud when unpacked from factory.

2-11. TRANSMIT INHIBIT OPTION. - The distant operator may request a close down of data communication by selecting "Inhibit Activate" (front panel switch). This sends the "Inhibit Activate" supervisory character which, &pending upon the strap option, is acted upon in one of two ways by the local AN/FYC-12. With option "A" selected in lights indicator "Inhibit RCVD" and, after completion of the character, automatically stops data communication. (The transmitter continues to send supervisory characters, which are not received by the distant sink terminal.) With option "B" selected, only the indicator "Inhibit RCVD" is lighted and the local operator must stop data communication manually. To re-open data communication, the distant operator must select "Inhibit Deactivate" on the front panel switch. This sends the "Inhibit Deactivate" supervisory character, extinguishes, the *'Inhibit RCVD" indicator, and starts data communications again. Determine which option is to be utilized for system operation. Use the card extractor to remove card assembly A2A3 (Inhibit Control Transfer Clock Generator). Figure 2-3 shows the location of the components on this card assembly. The strap option (P1) is located at the lower front end of the card. For option "A, " pin 7 and pin 8 should be connected and pin 14 and pin 1 open. For

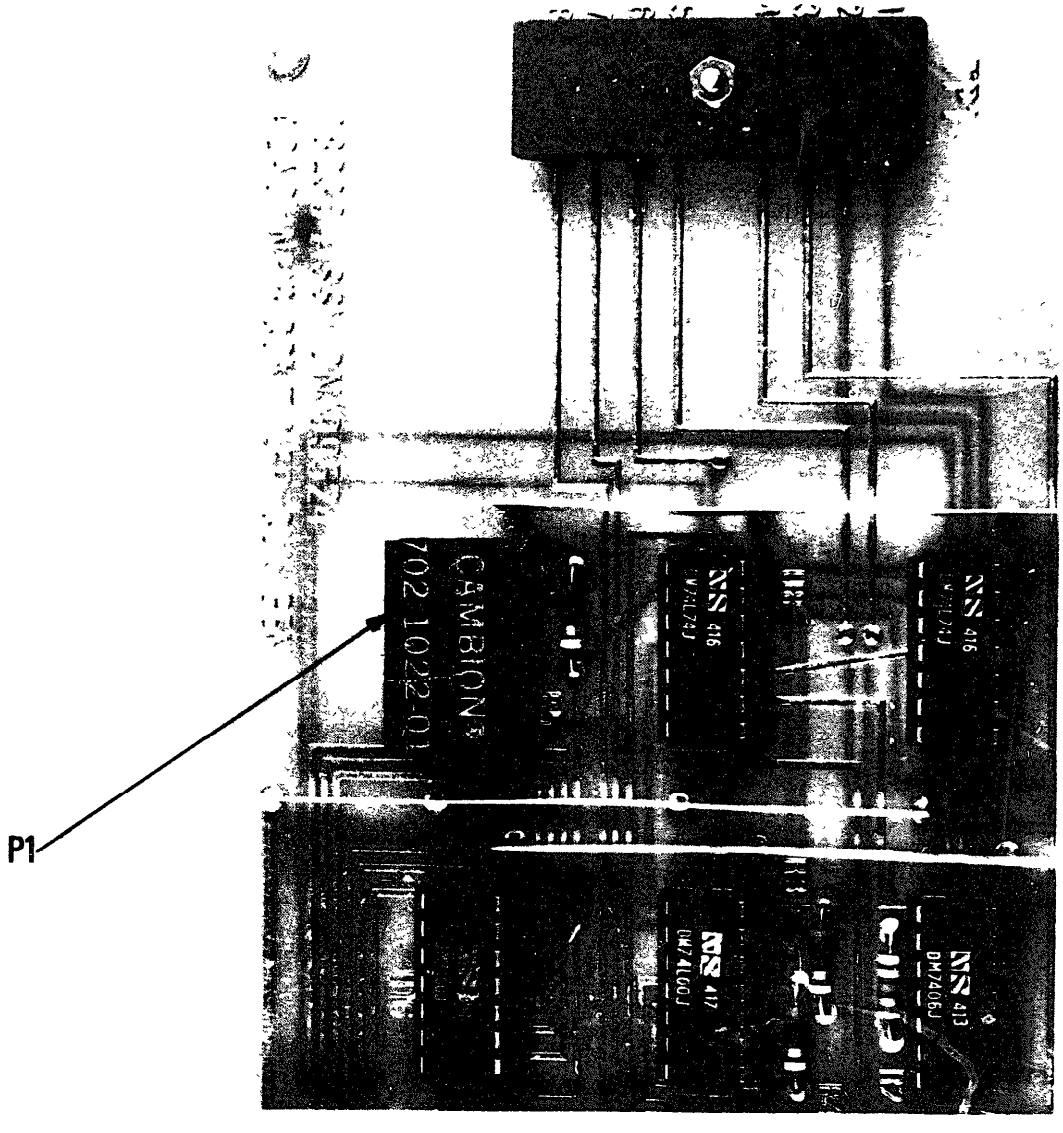


Figure 2-3. Inhibit Control Transfer Clock Generator Assembly A2A3

option “B” pin 14 and pin 1 are connected and pin 7 and pin 8 are open. Use the test meter to determine the option selected and reverse plug P1 to change the option if desired (reverse plug end to end). Make sure the plug is securely in its socket; then replace assembly A2A3. The transmit inhibit option is now set as required.

2-12. MEMORY LENGTH SELECTION. - The memory length of the AN/FYC-12 is adjusted by a 16-position thumbwheel switch S1-D, located on the setup panel, Figure 2-4. The memory length can be adjusted from eight characters (position 1) to 64 characters (position 15). Each step of the memory length switch increases memory length by four characters. Before adjusting the “Memory Length Switch” (S1-D), the round trip delay between the local and distant AN/FYC-12 must be determined. This delay depends upon the distance (miles) between the two stations, the data rate (baud), and the input data format and propagation velocity. It can be calculated from the following formula:

$$\text{Delay Characters} = \frac{\text{Twice Distance (Miles) x Baud Rate}}{\text{Propagation Velocity (Miles/sec) x Bits/Character}} + \text{six}$$

Table 2-4 illustrates the memory switch setting for distance to 8750 miles. The memory length selected should be one “Memory Length Switch” position greater than the calculated memory length. Thus, the minimum memory length is eight characters, or position 1 on thumbwheel switch S1-D. The six-character constant is due to character delays in AN/FYC-12 Data Sets, and data transmission modems used as part of the data communications link. The memory length must be adjusted with respect to the “Data Communications Link” and both ends of the data link (local and distant AN/FYC-12) must have the same memory length selected. Do not make memory length longer than required, or time will be lost t at every ARQ cycle, reducing communication throughout. If memory length is too short, the system fails to leave the ARQ cycle after detecting the first error. After determining the proper memory length, determine the switch position required and adjust the thumbwheel switch S1-D at both ends of the data link (local and distant). The thumbwheel switch is on a bracket located behind the control panel (refer to Figure 2-4).

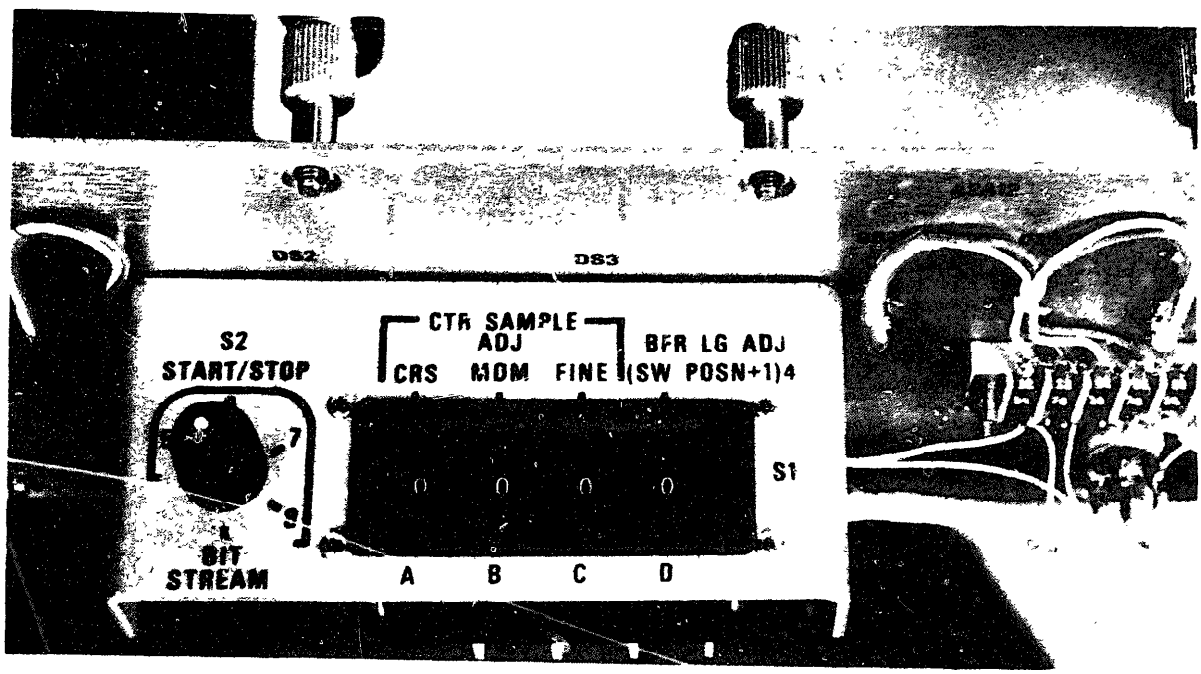


Figure 2-4. AN/FYC-12 Setup Controls

Table 2-4. Memory Length Switch Setting

Distance (Miles)	Memory Length Switch Setting (Assumed Free Space Velocity 186,000 miles/sec)															
	5-Bit S-S Bit Stream								6-Bit S-S				7-Bit S-S		8-Bit S-S	
	Data Rate (Baud)								Data Rate (Baud)							
	75	150	300	600	1200	2400	4800	9600	75	150	300	600	1200	2400	4800	9600
100	1								1							
200	1							2	1							
300	1							2	1							2
400	1						1		1							2
500	1						2	3	1						2	
600	1						2	3	1						2	
700	1					2		3	1						2	3
800	1					2		4	1					2		3
900	1					2		4	1					2		3
1000	1				2	3		4	1					2		3
1100	1				2	3		5	1					2		4
1200	1				2	3		5	1					2		4
1300	1				2		3	5	1					2	3	4
1400	1				2		3	6	1					2	3	4
1500	1				2		4	6	1					2	3	5
1600	1				2		4	6	1					2	3	5
1700	1				2		4	6	1					2	3	5
1800	1				2		4	7	1				2		3	5
1900	1				2	3	4	7	1				2		3	5
2000	1				2	3	4	7	1				2		3	6
2100	1				2	3	4	8	1				2		3	6
2200	1				2		3	5 8	1				2		4	6

Table 2-4 (Continued)

Distance (Miles)	Memory Length Switch Setting (Assumed Free Space Velocity 186,000 miles/sec)															
	5-Bit S-S Bit Stream								6-Bit S-S				7-Bit S-S		8-Bit S-S	
	Data Rate (Baud)								Data Rate (Baud)							
	75	150	300	600	1200	2400	4800	9600	75	150	300	600	1200	2400	4800	9600
2300	1				2	3	5	8	1				2		4	6
2400	1				2	3	5	9	1				2		4	7
2500	1			2		3	5	9	1				2		4	7
2750	1			2		3	5	10	1				2	3	4	8
3000	1			2		3	6	11	1				2	3	5	8
3250	1			2		4	6	11	1				2	3	6	9
3500	1			2		4	7	12	1			2		3	5	9
3750	1			2	3	4	7	13	1			2		3	5	10
4000	1			2	3	4	7	14	1			2		3	6	10
4250	1			2	3	4	8	15	1			2		3	6	11
4500	1			2	3	5	8	--	1			2		4	6	12
4750	1			2	3	5	9	--	1			2		4	7	12
5000	1		2		3	5	9	--	1			2		4	7	13
5250	1		2		3	5	9	--	1			2	3	4	7	13
5500	1		2		3	5	10	--	1			2	3	4	7	14
5750	1		2		3	6	10	--	1			2	3	4	8	14
6000	1		2		3	6	11	--	1			2	3	5	8	15
6250	1		2		4	6	11	--	1			2	3	5	8	--
6500	1		2		4	6	11	--	1			2	3	5	9	--
6750	1		2		4	6	12	--	1			2	3	5	9	--
7000	1		2		4	7	12	--	1		2		3	5	9	--
7250	1		2		4	7	13	--	1		2		3	5	10	--

Table 2-4 (Continued)

Distance (Miles)	Memory Length Switch Setting (Assumed Free Space Velocity 186,000 miles/sec)															
	5-Bit S-S Bit Stream								6-Bit S-S		7-Bit S-S		8-Bit S-S			
	Data Rate (Baud)								Data Rate (Baud)							
	75	150	300	600	1200	2400	4800	9600	75	150	300	600	1200	2400	4800	9600
7500	1		2	3	4	7	13	--	1		2		3	5	10	--
7750	1		2	3	4	7	13	--	1		2		3	6	10	--
8000	1		2	3	4	7	14	--	1		2		3	6	10	--
8250	1		2	3	4	8	14	--	1		2		3	6	11	--
8500	1		2	3	4	8	15	--	1		2		3	6	11	--
8750	1		2	3	5	8	15	--	1		2		4	6	11	--

2-13. SELECTION OF DATA FORMAT. - The Digital Data Set AN/FYC-12 is designed to operate with five different types of terminal equipment, or input formats:

1. Bit Stream
2. S-Bit Start-Stop
3. 6-Bit Start-Stop
4. 7-Bit Start-Stop
5. 8-Bit Start-Stop

The type of terminal equipment (format) is selected by the format switch S2, which is located on the set-up panel (Figure 2-4). After determining terminal equipment in use for the "Data Communication Link", set format switch S2 on setup panel on local and distant AN/FYC-12 accordingly. If the data format is any of the Start-Stop modes, the input data is automatically center sampled using the start bit as a reference, and the next section can be ignored.

2-14. CENTER SAMPLING

a. Operation of Center Sample Switch. - If the input format switch S2 is set to BIT STREAM, center bit sampling is accomplished by adjusting three 16-position thumbwheel switches S1-A, S1-B and S1-C located on the setup panel, (Figure 2-4). The three switches control the phase of the sampling clock in the AN/FYC-12. Switch S1-A is for coarse adjustment with a delay of 1.6 milliseconds per switch position; switch S1-B is for medium adjustment with a delay of 0.1 milliseconds per switch position; switch S1-C is for fine adjustment with a delay of 0.0065 milliseconds per switch position. The phase change generated by S1-A, S1-B, and S1-C is constant for all data rates (baud); therefore, different sections of the switch are used for different data rates. See Table 2-5, which shows the resolution of the coarse, medium, and fine switches with respect to data rate. At a data rate of 75 baud, a bit time is 13.33 milliseconds. Because the resolution of the coarse dial is 1.6 milliseconds per position, eight clicks of the coarse switch move the data sample clock from one end of the data pulse to the other. Hence the coarse setting is so adjusted that the data sample clock is positioned slightly before the pulse center and the medium adjustment can be used to center the pulse exactly. The fine adjustment has negligible effect at this data rate. At a data rate of 9600 baud, where a bit is 104 microseconds, the coarse contro1 is left at the zero position, since one click would move the sample point 16 bits. Hence, only the medium and fine adjustments need be used for center sampling.

Table 2-5. Center Sampling Adjustment

Data Rate (Baud)	Bit Period (Microsec.)	Center Sample Switch		
		Coarse (Sl-A)	Medium (S1-B)	Fine (S1-C)
		Clicks/Bit	Clicks/Bit	Clicks/Bit
75	13,333	8	---	---
150	6,666	4	---	---
300	3,333	2	---	---
600	1,667	1	16	---
1200	838	---	8	---
2400	417	---	4	---
4800	208	---	2	---
9600	104	---	1	16

b. Adjustment of Center Sample Switch. - To adjust the Center Sample Switch arrange to have the data terminal send a fixed data pattern--preferably a repeated mark-space. Power up the AN/FYC-12 and set CTR SAMPLE ADJ switches CRS, MDM, and FINE to zero. Monitor test points A2A1TP3 (X SP CLK) on Data Sample Generator assembly A2A1 and A2A6TP2 (X IN DA DL) on Data Input Code RAM Control A2A6. Use a dual channel oscilloscope such as the Tektronix Model 531, or equivalent. Connect channel one to A2A6TP2. This is the incoming data signal after it has been retimed. Use external synchronization from A2A2TP8 (X BIT LAST) on Fast Clock Step Generator A2A2. (X BIT LAST occurs once per character.) Figure 2-5 shows the signal X IN DA DL when a mark-space pattern is sent by the data terminal. Connect channel two to A2A1TP3. This is the clock wave form that samples the incoming data bits; it must be adjusted so that the clock pulses occur at the center of each data bit. The clock waveform for one character (eight bits) is illustrated in Figure 2-6. Adjust the center sample adjustment switches CRS, MDM, and FINE so that the transmitter serial/parallel clock (X SP CLK) falls at the center of each input data bit. Referring to Table 2-5, determine which thumbwheel to adjust. Start with the CRS switch (S1 -A) if the baud rate is 300 or less; start with the MDM switch (S1-B) if the baud rate is between 1200 and 4800; start with the FINE switch (S1-C) if the baud rate is 9600. Adjust the serial-to-parallel clock to be slightly before the center of the data bit on the first adjustment, and use the next lower resolution switch to finalize the adjustment. The correct adjustment is illustrated in Figure 2-7.

Note The transmitter serial/parallel clock pulses are only 3 microseconds wide and difficulty in viewing the clock pulses may be encountered at low baud rates.

When the center sampling adjustment has been accomplished all the preliminary adjustments are complete.

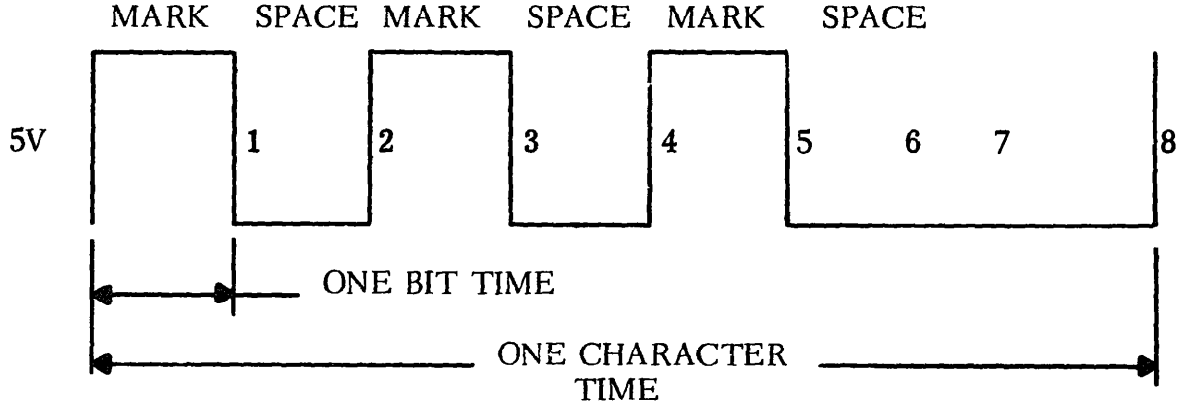


Figure 2-5. Bit Stream Data Input

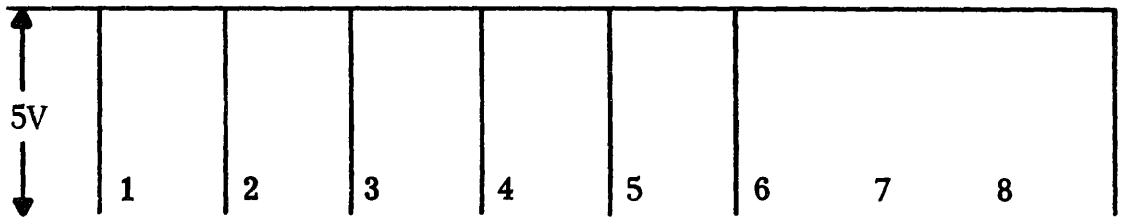
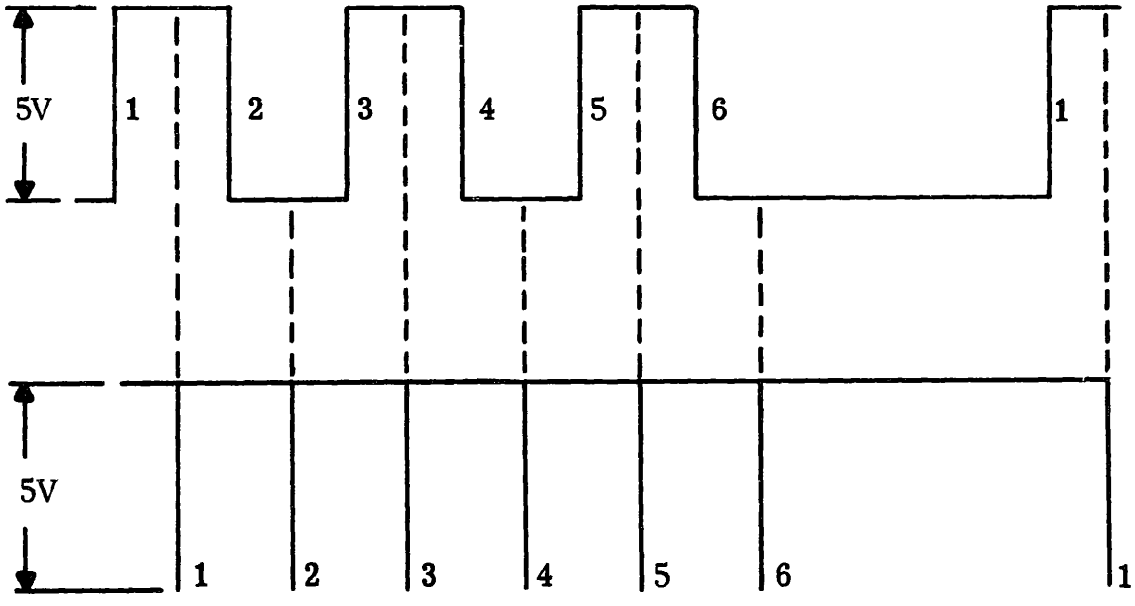


Figure 2-6. Transmitter Serial/Parallel Clock

INPUT DATA TP-4 ON A2A1



SERIAL-TO-PARALLEL CLOCK TP-3 ON A2A1

Figure 2-7. Correct Setting for Center Sample Switch

2-15. INSTALLATION TESTS. - Perform the tests specified in Chapter 5, Section II, Operational Tests and Optimum Performance. After testing is completed, securely fasten all front panel captive screws.

IV - PACKING AND STORAGE

2-16. PACKING PROCEDURES. - Check to see that all replaceable modules (A2A1 through A2A11 and A2A17) are securely fastened in the unit. Close front panel and tighten the captive front panel fasteners. To remove the unit from its installed position reverse the installation procedures listed in Section II of this chapter. Preservation, packing, and packaging of the unit for reshipment shall be in accordance with specification MIL-E-1755G The following portions of this specification are applicable:

1. Preservation and packaging (overseas shipment) - Level A, paragraph 3.1.1.
2. Preservation and packaging (domestic shipment) - Level C, paragraph 3.1.2.
3. Packing (overseas shipment) - Level A paragraph 3.2.1.
4. Packing (domestic shipment) - Level C, paragraph 3.2.4.
5. Marking, paragraph 3.12.

The equipment shall not be identified on the outer container and all other marking will be in accordance with MIL STD 129. Basically the unit is placed in an oversize container and cushioned with cellulose, especially around the front panel to protect the operating controls. It is protected from moisture by desiccants and enclosed in a sealed evacuated barrier bag. If the unit is shipped overseas, it should be blocked securely. Finally, it is placed in an outer container with bound cushioning.

2-17. STORAGE. - The Digital Data Set AN/FYC-12 can be stored in a sheltered environment within the limitations specified in Section III of Chapter 1. Under these conditions the conduit openings shall be sealed and the rear cover installed. For any other environmental conditions, the unit shall be prepared for shipment as specified in paragraph 2-16.

CHAPTER 3

OPERATING INSTRUCTIONS

I - CONTROLS AND INDICATORS

3-1. IDENTIFICATION OF CONTROLS AND INDICATORS. - All operator controls and indicators associated with Digital Data Set AN/FYC-12 are located on the front panel A2A12. Controls that are considered setup controls (those which are not utilized during normal operation once the equipment has been installed and checked out) are located on a bracket behind A2A12. To adjust these, the front panel fasteners must be loosened and the front panel opened on its hinges. Table 3-1 lists all the controls and indicators in alpha-numeric sequence by reference designations. Setup controls are indicated by an asterisk next to the reference designations. The table lists the names of each control or indicator as it appears on the front panel and states its function. Figure 3-1 shows the front panel controls, and Figure 3-2 the setup controls to which Table 3-1 refers.

Table 3-1. Controls and Indicators

REFERENCE DESIGNATION		CONTROL OR INDICATOR	FUNCTION
A2	CB1	POWER switch (circuit breaker) (Figure 3-1)	Energizes AN/FYC-12 with ±6 volts power and protects from overload.
Indicator Lamps (See Figure 3-1)			
A2A12	DS1	POWER ON	Illuminated when AN/FYC-12 is energized.
A2A12	DS2	SYNC	Illuminated when AN/FYC-12 is in sync cycle.
A2A12	DS3	ARQ	Illuminated when AN/FYC-12 is in ARQ cycle.

Table 3-1 (Continued)

REFERENCE DESIGNATION		CONTROL OR INDICATOR	FUNCTION
A2A12	DS4	MUT CHAR	Illuminated when AN/FYC-12 receiver detects Invalid Character.
A2A12	DS5	PARITY FAIL	Illuminated when a memory error in internal memory is detected.
A2A12	DS6	INHIBIT REQ	Illuminated when either local inhibit switch (S5) or remote input local inhibit is activated.
A2A12	DS7	INHIBIT RCVD	Illuminated when AN/FYC-12 receiver detects "Inhibit Activate" character.
A2A12	DS8	TEST	Illuminated when system test switch (S6) is in test position.
*Setup Control Switches (See Figure 3-2)			
A2A12	S1A*	CTR SAMPLE ADJ (CRS)	3-section thumbwheel switch to set up center bit sampling in bit stream mode.
	S1B*	CTR SAMPLE ADJ (MDM)	Section A - Coarse B - Medium C - Fine
	S1C*	CTR SAMPLE ADJ (FINE)	
A2A12	S1D*	BFR LG ADJ	16-position thumbwheel switch which controls the length of transmitter memory.

Table 3-1 (Continued)

REFERENCE DESIGNATION		CONTROL OR INDICATOR	FUNCTION
A2A12	S2*	(Data Format Switch)	S-position rotary switch which determines the input data format of AN/FYC-12. The positions are: START/STOP 5 5-Bit Start/ stop START/STOP 6 6-Bit Start/ stop START/STOP 7 7-Bit Start/ stop START/STOP 8 8-Bit Start/ stop BIT STREAM Bit Stream
Control Switches (See Figure 3-1)			
A2A12	S3	SYNC	Momentary action pushbutton switch which initiates a sync cycle providing system is in ARQ cycle.
A2A12	S4	PARITY FAIL	Momentary action pushbutton switch which resets PARITY FAIL indicator.
A2A12	S5	INHIBIT ACTIVATE/ DEACTIVATE	Two-position toggle switch to enable “Inhibit Activate” supervisor character to be transmitted. Normal operating position is INHIBIT - DEACTIVATE.

Table 3-1 (Continued)

REFERENCE DESIGNATION		CONTROL, OR INDICATOR	FUNCTION
A2A12	S6	TEST	Two-position toggle switch to enable test mode selection. Normal operating position is OFF. CAUTION. -If this switch is operated in normal communications then data and synchronization may be lost to the distant end.

II - OPERATING PROCEDURES

3-2. TURN ON PROCEDURE. - To turn on the equipment after the normal system operating mode has been established, turn power switch to ON and observe the status of front panel indicators. Depress the PARITY FAIL switch to extinguish the PARITY FAIL lamp. If the local AN/FYC-12 is synchronized with the distant AN/FYC-12, all panel lights should be extinguished and normal system operation exists. If the system is not synchronized the MUT CHAR (Mutilated Character) and ARQ lamps are lighted. Depress the SYNC button to initiate a sync cycle. The SYNC lamp lights, the mutilated character lamp is extinguished: and finally. the ARQ and SYNC lights are extinguished. At this time the local system is synchronized, and data can be sent normally to the distant system. If the distant system is operating normally, full duplex operation is established: and messages can be sent in both directions. During normal operation the MUT CHAR and ARQ lamps light, when the receiver receives an invalid character from the distant transmitter; and the local transmitter puts out a request for automatic retransmission of data (ARQ) from the far end, The lamps extinguish when normal data flow is re-established. The frequency of this occurrence depends upon many factors, normally outside the local Digital Data Set AN/FYC-12. If, upon power turn-on, synchronization (normal operation) cannot be established, proceed with paragraph 3-3.

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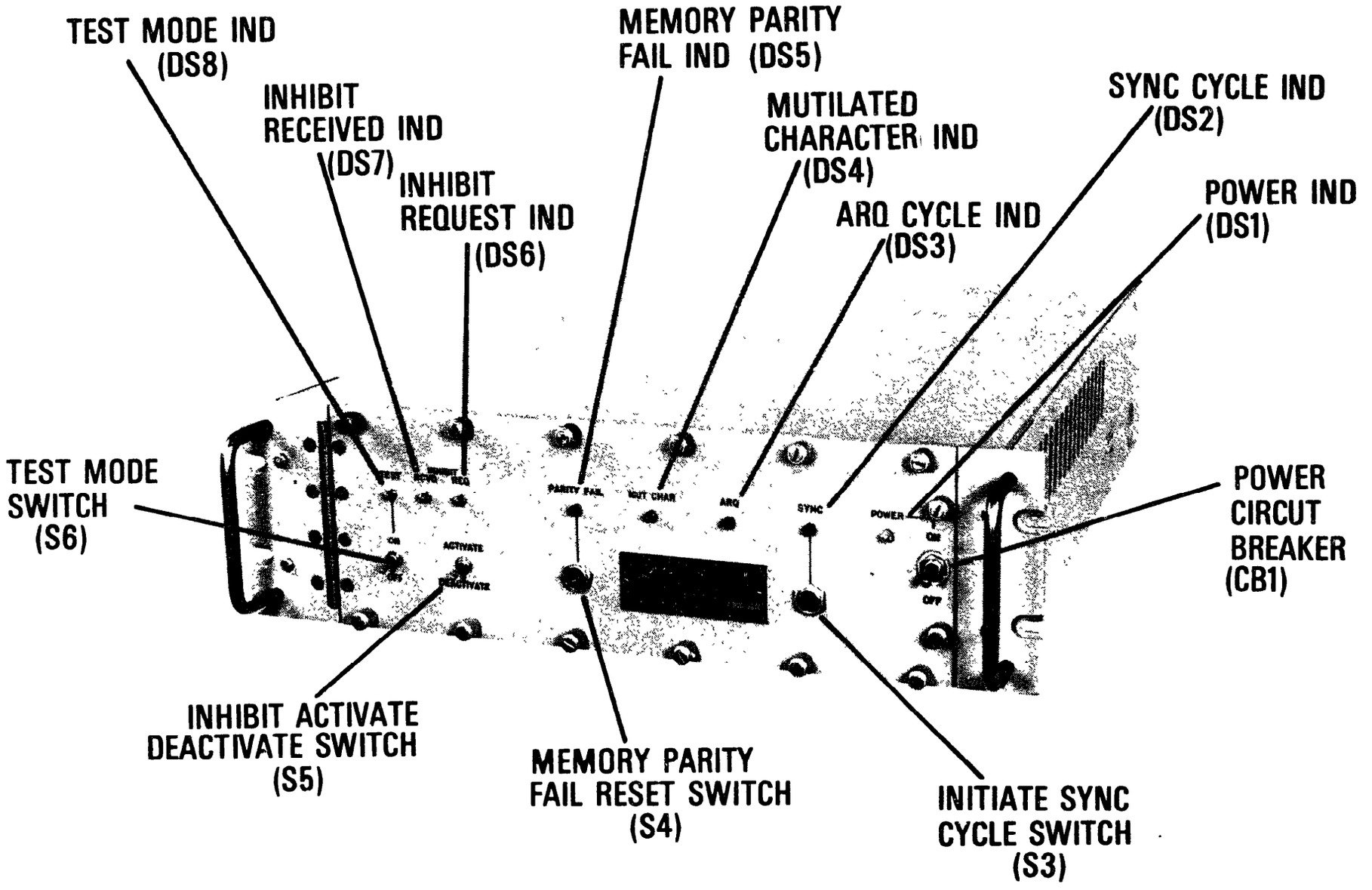


Figure 3-1. AN/FYC-12 Operating Controls and Indicators

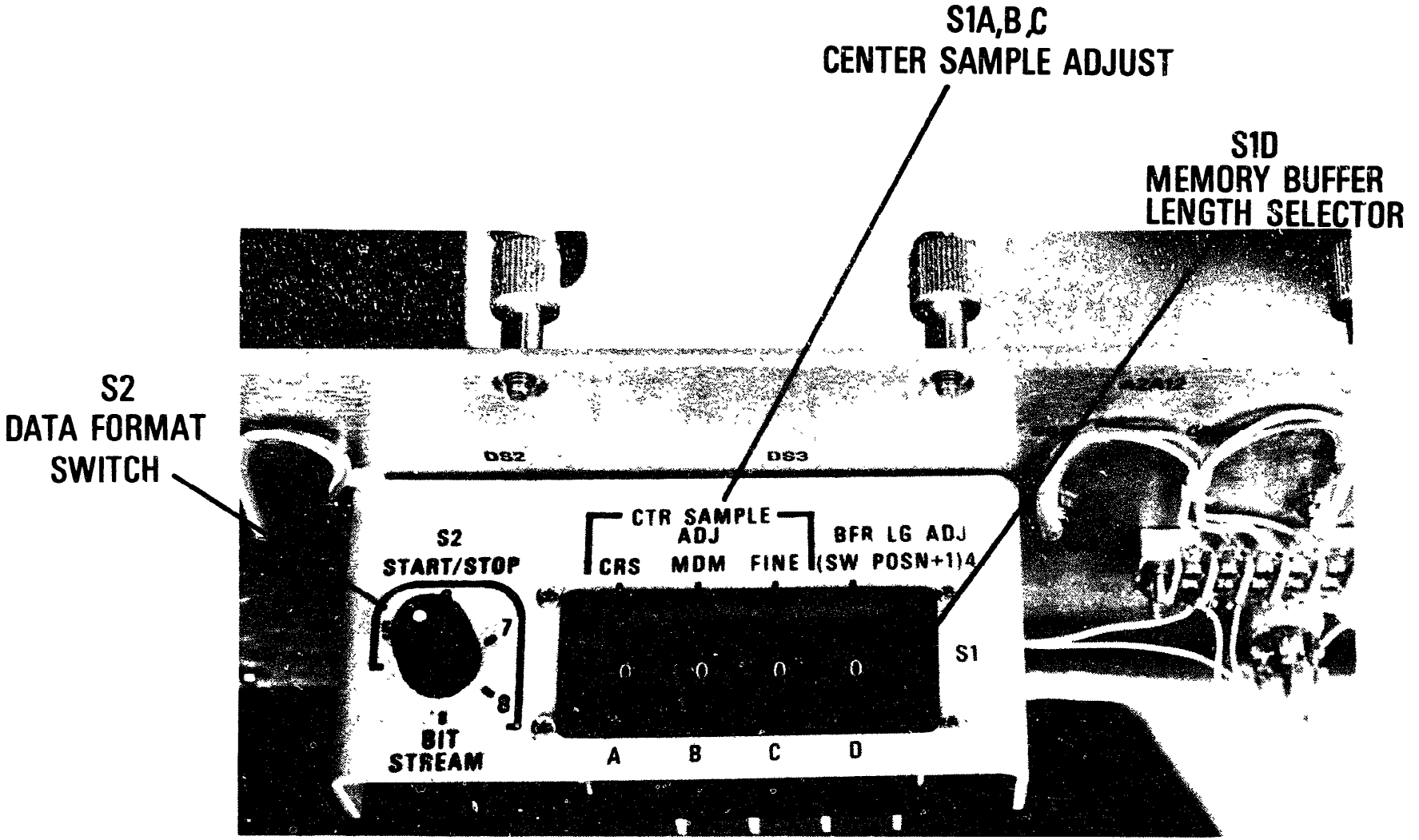


Figure 3-2. AN/FYC-12 Setup Controls

3-3. PRE-OPERATIONAL PROCEDURES. - If normal operation cannot be established, place TEST switch in ON position. The TEST lamp should light along with the MUT CHAR and ARQ lamps. Depress the SYNC button and initiate a sync cycle. If unit synchronizes (SYNC lamp lights; then MUT CHAR, ARQ lamps, and finally the SYNC lamp extinguish)) men the difficulty lies either in faulty format or memory length selection, or a problem with the communications modem. If the unit fails to synchronize, check for presence of input data at TB3-1 and 2, and transmit clock at TB3-4 and 3. If both are present, proceed with corrective maintenance in accordance with Chapter 6. If the unit synchronizes in the test mode, place TEST switch to OFF and re-check the procedures of Chapter 2, Section III, Adjustments. These include the following paragraphs:

2-13	Selection of data format,
2-12	Memory length selection,
2-10	Line driver capacitor selection, and
2-14	Center sampling adjustment (bit stream operation only).

Improper selection of the data format and selection of too small an amount of data storage results in the inability to synchronize the system. Using incorrect values of output capacitance and improper adjustment of center sampling in bit stream operation can cause timing problems that lead to marginal or improper system operation. If operation of the system appears normal in the test mode, the above adjustments have been completed, and the unit still fails to synchronize when the SYNC button is depressed, the problem is outside the local AN/FYC-12. Check input and output connections at the AN/FYC-12 interface, the communications modem, and the distant AN/FYC-12 for faulty operations,

3-4. OPERATING PROCEDURES. - The normal operation of the Digital Data Set is dictated by system operating procedures outside the scope of this manual. In general, there should be no need to operate any switches other than the Parity Reset Switch S-4, If the MUT CHAR and ARQ lamps are lit con -- stantly, the system is unsynchronized. Synchronization can be initiated at either end of the communication link, at the front panel or by remote control. It should be noted that the normal position of the TEST switch is the OFF position. Unauthorized placement of the equipment in the test mode causes the destruction of the data in the transmitter memory.

3-5. SHUT DOWN PROCEDURE. - The equipment should not be turned off until system operating procedures dictate that it must be brought off line for maintenance. Once the system is off line, turn the power switch to the OFF position to shut down the equipment.

CHAPTER 4

PRINCIPLES OF OPERATION

I - BASIC PRINCIPLES

4-1. GENERAL. - Logic modules used in the AN/FYC-12 are integrated circuits packaged in 14- and 16-pin dual in -line cases. Logic symbols and truth tables for these circuits appear in Figures A-l through A-24, and case diagrams, including voltage connections for the 14-pin and 16-pin packages, are shown in Figure A -25 unless otherwise noted on individual drawings. On the more complex logic modules, data inputs are indicated by letters or by alphanumerics, and data outputs are indicated by numbers. Control inputs are shown as letters, letter combinations, or alphanumerics. Counter outputs are indicated as 1, 2, 4, 8; shift register outputs are indicated as 1, 2, 3, 4.

4-2. DEFINITIONS.

a. TTL Logic Modules. - The twenty-four TTL logic modules shown in Figures A-l through A -24 are briefly defined as follows:

(1) Hex Inverters (Figure A-l). - This package contains six identical inverter blocks, which may be used as logical inverters or as buffer amplifiers to increase the fan-out of any signal.

(2) Quad Two-Input NAND Gate (Figure A-2). - This package contains four identical two-input NAND gates. Both inputs must be HIGH to make the output LOW.

(3) Quad Two-Input NOR Gate (Figure A-3). - This package contains four identical two-input NOR gates. Either or both inputs must be HIGH to make the output LOW.

(4) Triple Three-Input NAND Gate (Figure A-4). - This package contains three identical three-input NAND gates. All three inputs must be HIGH to make the output LOW.

(5) Triple Three-Input NOR Gate (Figure A-5). - This package contains three identical three-input NOR gates. Any or all inputs must be HIGH to make the output LOW.

(6) Dual Four-Input NAND Gate (Figure A-6). - This package contains two identical four-input NAND gates. All four inputs must be HIGH to make the output LOW.

(7) Dual Four -Input NOR Gate (Figure A -7). - This package contains two identical four-input NOR gates. Any or all inputs must be HIGH to make the output LOW.

(8) Single Eight-Input NAND Gate (Figure A-8). - This package contains one eight-input NAND gate. All eight inputs must be HIGH to make the output LOW.

(9) Dual Two Wide, Two-Input AND-OR-INVERT Gates (Figure A-9). - This package contains two identical AND-OR-INVERT gates. If either of the two NAND gates has both inputs HIGH, the output is LOW.

(10) 4-Bit Magnitude Comparator (Figure A-10). - This package compares a 4-bit word (A) with a second 4-bit word (B). It has three output pins that will be HIGH when A = B, or A> B, or A< B. It is also capable of being expanded to compare n-bit words.

(11) 9-Bit Odd/Even Parity Generator//Checker (Figure A-11). - This package generates or checks odd or even parity of an 8-bit word. It is capable of being expanded to generate or check parity of n-bit words.

(12) Dual Interface Transmitter (Figure A-12). - This package con - tains two identical line driver circuits that convert TTL signal levels (0V = LOW and 5V = HIGH) into bi-polar levels required by low level dc interface (MIL STD 188C) +6V = HIGH and -6V = LOW.

(13) Dual Interface Receiver (Figure A-13). - This package contains two identical line receiver circuits that convert low level dc interface levels (+6V = HIGH and -6V = LOW) into TTL signal levels (0V = LOW and +5V = HIGH).

(14) Dual D-Type Flip-Flop with Preset and Clear (Figure A-14). - This package contains two identical D-type flip-flops. The signal level on input D is transferred to the output on the rise of the clock signal. The device can be changed asynchronously with the preset and reset inputs.

(15) Dual J-K Flip-Flop with Clear (Figure A-15). - This package contains two identical J-K flip-flops. The signal level on input J or K is trans - ferred to the output on the fall of the clock. If J and K inputs are both HIGH, the device toggles; if both are LOW, the output does not change. The device can be reset asynchronously with the reset input.

(16) Dual J-K Flip-Flop with Clear (Figure A-16). - This package contains **two** identical J-K (master-slave) flip-flops similar to those of Figure A-15.

(17) Dual T-K Flip-Flop with Preset and Clear (Figure A-17). - This package contain; two identical J-K flip-flops with preset and reset. It functions the same as the device of Figure A-15, except that it can be asynchronously preset as well as reset, and has a data lock provision to simplify logic design.

(18) Synchronous 4-Bit Counter (Figure A-18). - This package contains a 4-bit synchronous binary counter. The counter can be preset to any 4-bit number, or reset to zero. Enable and look-ahead carry features allow cascading devices into counts of n-bits.

(19) Synchronous Up/Down Counter (Figure A-19). - This package contains a 4-bit synchronous up/down binary counter. The counter is similar to Figure A-18 except that it is able to add or subtract counts from the total. Also, the programmable load, which presets output to any 4-bit number is asynchronous.

(20) 4-Bit Parallel-Access Shift Register (Figure A-20). - This package contains a 4-bit parallel-access shift register. The 4-bit word can be parallel loaded and then serially shifted to form serial output. It can be cascaded to increase the word length.

(21) 8-Bit Parallel-Out Serial Shift Register (Figure A-21). - This package contains an 8-bit shift register featuring gated serial inputs and an asynchronous clear. Data at the serial inputs can be changed while the clock is high and data is shifted on the rise of clock.

(22) 256-Bit Read/Write Memory (Figure A-22). - This package contains 256 single bits of read/write memory. The address locations are provided by an 8-bit binary address. The output of the memory is the complement of the input.

(23) 64 Bit Read Write Memory (Figure A-23). - This package contains 16 x 4-bit words of read/write memory. The 16 address locations are provided by a 4-bit binary address. The package is also equipped with a chip-select input to expand the memory length. The output of memory is the complement of the input.

(24) 256 x 4-Bit Read Only Memory (Figure A-24). - This package contains 256 x 4-bit words of read only memory. The 256 address locations are provided by an 8-bit binary address. Five tables are given to show the 4-bit word at each address in the five types of packages used in the AN/FYC-12.

b. Constant Ratio Codes. - The AN/FYC-12 uses a constant ratio code to transmit the communication to the distant receiver. This type of code always has the same number of l's for each code and can be used to detect errors in

transmission. The AN/FYC-12 utilizes a constant ratio code with four l's in every character transmitted. The number of possible combinations in a constant ratio code of this type, with four 1's in each code and a total of X Bits, is given by:

$$\text{Code Combinations} = \frac{x!}{4! \times (x - 4)!}$$

The AN/FYC-12 is designed to operate with a maximum of 256 code combinations (8-bit start-stop) and a minimum of 32 code combinations (5-bit start-stop); to optimize the system two lengths of constant ratio code are used. Eight bits per character provide 70 combinations for bit stream and S-bit start-stop. Eleven bits per character provide 330 combinations for 6-, 7-, and 8-bit start-stop. Not all constant ratio code combinations are used in every input format. In the AN/FYC-12 receiver, the unused codes and the nonconstant ratio codes are declared invalid.

c. Supervisory Characters. - In addition to normal data communication characters, the AN/FYC-12 uses six supervisory characters to control and synchronize the error detection and correction system. The constant ratio codes for these characters, for each of the code lengths, are shown in Table 4-1.

Table 4-1. Supervisor Control Characters

Supervisor	Constant Ratio Code
8 Bit Format	
IDLE	10100110
ARQ	11100010
SYNC A	00001111
SYNC B	11110000
INHIBIT ACTIVATE	11100100
INHIBIT DEACTIVATE	11101000
11 Bit Format	
IDLE	00010100110
ARQ	00011100010
SYNC A	00000001111
SYNC B	11110000000
INHIBIT ACTIVATE	00011100100
INHIBIT DEACTIVATE	00011101000

The characters perform the following tasks:

(1) IDLE. - Transmitted when no response is made by data source to clock step (start-stop modes only).

(2) ARQ. - Request retransmission from the transmitter memory.

(3) SYNC A, SYNC B. - Always transmitted as a pair to give unique sequence of eight l's which is recognized at any bit time by the distant receiver and used to resynchronize the system.

(4) INH ACTIVATE. - Transmitted to control the distant terminal. The AN/FYC-12 has a strap option that changes the action taken on receiving INH ACTIVATE. With option A, the distant source closes down and the INHIBIT RCVD lamp is lighted. With option B, only the indicator INHIBIT RCVD lamp is lighted.

(5) INH DEACTIVATE. - Transmitted to restart the distant source and extinguish the INHIBIT RCVD indicator. _

d. Input Data Formats. - The AN/FYC-12 is designed to operate with five different types of terminal equipment at data rates between 75 and 9600 baud. The input data formats are: Bit Stream, S-bit start-stop, 6-bit start-stop, 7-bit start-stop and 8-bit start-stop. The Data Format switch (S2) selects the type of input format and hence the length of the constant ratio code in use by the system.

(1) Bit Stream. - In the bit stream mode the data being communicated is continuous with no character boundaries, start bits, or stop bits. The AN/FYC-12 reads six bits for each constant ratio code and uses an 8-bit constant ratio code with 70 different combinations. The six input bits have 64 combinations, which are encoded by the AN/FYC-12 transmitter into constant ratio codes as shown in Table 4-2. With the six supervisory characters required there are no unused codes.

(2) 5-Bit Start-Stop. - In all start-stop modes a start bit and at least one stop bit are added to each character to enable the distant data sink to self synchronize. In 5 bit start-stop format the AN/FYC-12 includes the start bit; which is always LOW, as part of the character code. The transmitter adds two entire LOW bits to the front end of the code and then encodes the 8-bit combination (first 3 bits always LOW) into an 8-bit constant ratio code for transmission to the distant receiver. In 5 bit start-stop there are 32 code combinations, and six control supervisor characters required by the AN/FYC-12, making a total of 38 different combinations. The 8-bit constant ratio code has 70 combinations leaving 32 unused in S-bit start-stop format. The constant ratio codes for the 32 S-bit combinations are shown in Table 4-3.

(3) 6-Bit Start-Stop. - In 6-bit start-stop format the AN/FYC-12 includes the start bit as part of the character code; the transmitter adds a single HIGH bit to the front end of the code and then encodes the 8-bit combination (first bit always HIGH and second bit always LOW) into an 11-bit constant ratio code for transmission to the distant receiver. In 6-bit start-stop there are 64 code combinations and the same six control supervisory characters, making a total of 70 different combinations. The 11-bit constant ratio code has 330 combinations leaving, 256 unused in the 6-bit start-stop format. The constant ratio codes for the 64 6-bit combinations are shown in Table 4-4.

(4) 7-bit Start-Stop. - In 7-bit start-stop format the transmitter also includes the start bit is make up an 8-bit combination (first bit always LOW), which it encodes into an 11-bit constant ratio code for transmission to the distan t receiver. In 7-bit start-stop there are 128 code combinations and six control supervisory characters making a total of 134 different combinations. The 11-bit constant ratio code has 330 combinations leaving 196 unused. The constant ratio codes for the 128 7-bit combinations are shown in Table 4-5.

(5) 8-Bit Start-Stop. - In 8-bit start stop format only the eight data bits are encoded by the transmitter into an 11-bit constant ratio code (the distant receiver adds the missing start bit before the character is sent to the data sink). In 8-bit start stop there are 256 code combinations, and six supervisory characters making a total of 262 different combinations and hence leaving 68 unused 11-bit constant ratio codes. The constant ratio codes for the 256 8-bit combinations are shown in Table 4-6.

e. Unused Constant Ratio Codes. - The number of constant ratio codes that are used by the AN/FYC-12 depends upon the input data format. Table 4-7 and 8 list the number of used and unused codes in each of the five data formats.

f. AR Cycle. - The purpose of the AN/FYC-12 is to detect transmission errors and automatically request a retransmission of the erroneous data se - quence. This operation--known as an ARQ cycle--closes down communications in both directions for one memory sequence, retransmitting the previously memorized data. To prevent returning to normal data flow with a random bit sequence input (containing some valid constant ratio codes) the receiver must receive two sequential ARQ supervisory characters before normal data flow can be resumed. The complete ARQ cycle is illustrated in Figure A-54.

g. SYNC Cycle. - The constant ratio codes used by the AN/FYC-12 are not serf synchronizing, and the distant receiver must be correctly synchronized to the local transmitter. If the system is not synchronized, the most likely reason is that it is in a constant ARQ cycle. If the same character or super-

visory character is transmitted repeatedly, the erroneous synchronization could mutilate the constant character into another valid constant ratio code, which would not produce an ARQ cycle. The operator initiates resynchronization by pressing the SYNC button (S3) at either the local or distant end of the system. This transmits the resynchronization sequence of eight 1's followed by four or seven O's (supervisory character SYNC: A followed by SYNC B) and a series of Inhibit Activate or Inhibit Deactivate supervisory characters, but does not change the data stored in the memory. The distant receiver recognizes the resynchronization pattern at any bit time and changes the receiver last bit time to be synchronized to the incoming data. The number of bits that the receiver last bit time is advanced or retarded is determined so that the receiver ARQ character counter can keep count of the number of characters transmitted. The system will not leave the resynchronization sequence until the distant receiver has correctly received the Inhibit Activate or the Inhibit Deactivate supervisory character. The above sequence is known as a SYNC cycle and is illustrated in Figure A -55.

h. Rates and Clocks. - The AN/FYC-12 may be operated at data rates between 75 and 9600 baud. It requires an external clock at twice the data rate for the transmitter and a synchronous, correctly phased, external clock for the receiver--also at twice the data rate. The transmitter generates a step clock in phase with the external clock to request a new data character. In bit stream mode this is six complete cycles of the transmitter clock and the data source must respond with one data bit for each cycle. In start-stop modes it is a single high pulse (+6V) for two bit times and the data source must respond with a complete character, including start and stop bits. The receiver also generates a step clock for the data sink in bit stream mode; it is also six cycles of the receiver clock and in phase with the output data bits. In start-stop the step clock is a single pulse (+6V) for one bit time marking the start bit of each character.

Table 4-2. Bit Stream

	Input Code	Constant Ratio Code
0	000000	11011000
1	000001	00010111
2	000010	00011011
3	000011	00011101
4	000100	00011110
5	000101	00100111
6	000110	00101011
7	000111	00101101
8	001000	00101110
9	001001	00110011
10	001010	00110101
11	001011	00110110
12	001100	00111001
13	001101	00111010
14	001110	00111100
15	001111	01000111
16	010000	01001011
17	010001	11100001
18	010010	01001110
19	010011	01010011
20	010100	01010101
21	010101	01010110
22	010110	01011001
23	010111	01011010
24	011000	01011100
25	011001	01100011
26	011010	01100101
27	011011	01100110

Table 4-2 (Continued)

	Input Code	Constant Ratio Code
28	011100	01101001
29	011101	01101010
30	011110	01101100
31	011111	01001101
32	100000	01110001
33	100001	01110010
34	100010	01110100
35	100011	01111000
36	100100	10000111
37	100101	10001011
38	100110	10001101
39	100111	10001110
40	101000	10010011
41	101001	10010101
42	101010	10010110
43	101011	10011001
44	101100	10011010
45	101101	10011100
46	101110	10100011
47	101111	10100101
48	110000	10101001
49	110001	10101010
50	110010	10101100
51	110011	10110001
52	110100	10110010
53	110101	10110100
54	110110	10111000
55	110111	11000011

Table 4-2 (Continued)

	Input Code	Constant Ratio Code
56	111000	11000101
57	111001	11000110
58	111010	11001001
59	111011	11001010
60	111100	11001100
61	111101	11010001
62	111110	11010010
63	111111	11010100

Table 4-3. 5-Bit Start-Stop

	Input Code	Constant Ratio Code
0	000000	11011000
1	000001	00010111
2	000010	00011011
3	000011	00011101
4	000100	00011110
5	000101	00100111
6	000110	00101011
7	000111	00101101
8	001000	00101110
9	001001	00110011
10	001010	00110101
11	001011	00110110
12	001100	00111001
13	001101	00111010
14	001110	00111100
15	001111	01000111
16	010000	01001011
17	010001	11100001
18	010010	01001110
19	010011	01010011
20	010100	01010101
21	010101	01010110
22	010110	01011001
23	010111	01011010
24	011000	01011100
25	011001	01100011
26	011010	01100101
27	011011	01100110

Start Bit

Table 4-3 (Continued)

	Input Code	Constant Ratio Code
28	(011100	01101001
29	011101	01101010
30	011110	01101100
31	011111	01001101

Table 4-4. 6-Bit Start-Stop

	Input code		Constant Ratio Code
0	1	/0000000	1001001001 0
1	1	0000001	1001001010 0
2	**1**	**0000010**	1001000101 0
3	1	0000011	1001000110 0
4	1	0000100	1001000011 0
5	1	0000101	1001000001 1
6	1	0000110	1000110001 0
7	1	0000111	1000110010 0
8	1	0001000	1000101001 0
9	1	0001001	1000101010 0
10	1	0001010	1000100101 0
11	1	0001011	1000100110 0
12	1	0001100	1000100011 0
13	1	0001101	1000100001 1
14	1	0001110	1000011001 0
15	1	0001111	1000011010 0
16	1	0010000	0101001001 0
17	1	0010001	0101001010 0
18	1	0010010	0101000101 0
19	1	0010011	0101000110 0
20	1	0010100	0101000011 0
21	1	0010101	0101000001 1
22	1	0010110	0100110001 0
23	1	0010111	0100110010 0
24	1	0011000	0100101001 0
25	1	0011001	0100101010 0
26	1	\0011010	0100100101 0

Start Bit

Table 4-4 (Continued)

		Start Bit	Input Code	Constant Ratio Code
27	1	/	0011011	010010011100
28	1		0011100	010010001110
29	1		0011101	010010000011
30	1		0011110	010001100010
31	1		0011111	010001101100
32	1		0100000	001100100010
33	1		0100001	001100101100
34	1		0100010	001100010110
35	1		0100011	001100011100
36	1		0100100	001100001110
37	1		0100101	001100000011
38	1		0100110	001011000010
39	1		0100111	001011001100
40	1		0101000	001010100010
41	1		0101001	001010101100
42	1		0101010	001010001010
43	1		0101011	001010011100
44	1		0101100	001010001110
45	1		0101101	001010000011
46	1		0101110	001001100010
47	1		0101111	001001101100
48	1		0110000	100001010110
49	1		0110001	100001011100
50	1		0110010	100001001110
51	1		0110011	100001000011
52	1		0110100	100000110110
53	1		0110101	100000011100

Table 4-4 (Continued)

		Input Code	Constant Ratio Code
54	1	0 1 1 0 1 1 0	1 0 0 0 0 0 1 0 1 1 0
55	1	0 1 1 0 1 1 1	1 0 0 0 0 0 1 0 0 1 1
56	1	0 1 1 1 0 0 0	1 0 0 0 0 0 0 1 1 1 0
57	1	0 1 1 1 3 0 1	1 0 0 0 0 0 0 1 0 1 1
58	1	0 1 1 1 0 1 0	1 1 0 1 0 0 1 0 0 0 0
59	1	0 1 1 1 0 1 1	1 1 0 0 1 0 1 0 0 0 0
60	1	0 1 1 1 1 0 0	1 1 0 0 0 1 1 0 0 0 0
61	1	0111101	1 0 0 1 1 0 1 0 0 0 0
62	1	0111110	1 0 0 1 0 1 1 0 0 0 0
63	1	0111111	1 1 0 1 1 0 0 0 0 0 0

Start Bit

Table 4-5. 7-Bit Start-Stop

	Input Code	Constant Ratio Code
0	00000000	00011011000
1	00000001	00000010111
2	00000010	00000011011
3	00000011	00000011101
4	00000100	00000011110
5	00000101	00000100111
6	00000110	00000101011
7	00000111	00000101101
8	00001000	00000101110
9	00001001	00000110011
10	00001010	00000110101
11	00001011	00000110110
12	00001100	00000111001
13	00001101	00000111010
14	00001110	00000111100
15	00001111	00001000111
16	00010000	00001001011
17	00010001	00011100001
18	00010010	00001001110
19	00010011	00001010011
20	00010100	00001010101
21	00010101	00001010110
22	00010110	00001011001
23	00010111	00001011010
24	00011000	00001011100
25	00011001	00001100011
26	00011010	00001100101
27	00011011	00001100110

Start Bit

Table 4-5 (Continued)

	Input Code	Constant Ratio Code
28	/ 0 0 0 1 1 1 0 0	0 0 0 0 1 1 0 1 0 0 1
29	0 0 0 1 1 1 0 1	0 0 0 0 1 1 0 1 0 1 0
30	0 0 0 1 1 1 1 0	0 0 0 0 1 1 0 1 1 0 0
31	0 0 0 1 1 1 1 1	0 0 0 0 1 0 0 1 1 0 1
32	0 1 0 0 0 0 0 0	0 0 0 0 1 1 1 0 0 0 1
33	0 1 0 0 0 0 0 1	0 0 0 0 1 1 1 0 0 1 0
34	0 1 0 0 0 0 1 0	0 0 0 0 1 1 1 0 1 0 0
35	0 1 0 0 0 1 1	0 0 0 0 1 1 1 1 0 0 0
36	0 1 0 0 1 0 0	0 0 0 1 0 0 0 0 1 1 1
37	0 1 0 0 1 0 1	0 0 0 1 0 0 0 1 0 1 1
38	0 1 0 0 1 1 0	0 0 0 1 0 0 0 1 1 0 1
39	0 1 0 0 1 1 1	0 0 0 1 0 0 0 1 1 1 0
40	Start Bit 0 1 0 1 0 0 0	0 0 0 1 0 0 1 0 0 1 1
41	0 1 0 1 0 0 1	0 0 0 1 0 0 1 0 1 0 1
42	0 1 0 1 0 1 0	0 0 0 1 0 0 1 0 1 1 0
43	0 1 0 1 0 1 1	0 0 0 1 0 0 1 1 0 0 1
44	0 1 0 1 1 0 0	0 0 0 1 0 0 1 1 0 1 0
45	0 1 0 1 1 0 1	0 0 0 1 0 0 1 1 1 0 0
46	0 1 0 1 1 1 0	0 0 0 1 0 1 0 0 0 1 1
47	0101111	0 0 0 1 0 1 0 0 1 0 1
48	0110000	0 0 0 1 0 1 0 1 0 0 1
49	0110001	0 0 0 1 0 1 0 1 0 1 0
50	0110010	0 0 0 1 0 1 0 1 1 0 0
51	0110011	0 0 0 1 0 1 1 0 0 0 1
52	0110100	0 0 0 1 0 1 1 0 0 1 0
53	0110101	0 0 0 1 0 1 1 0 1 0 0
54	0110110	0 0 0 1 0 1 1 1 0 0 0
55	0110111	0 0 0 1 1 0 0 0 0 1 1

Table 4-5. (Continued)

	Input Code	Constant Ratio Code
56	0111000	00011000101
57	0111001	00011000110
58	0111010	00011001001
59	0111011	00011001010
60	0111100	00011001100
61	0111101	00011010001
62	0111110	00011010010
63	0111111	00011010100
64	01000000	11100000100
65	01000001	11100000010
66	01000010	11010100000
67	01000011	11011000000
68	01000100	10011100000
69	01000101	10000000111
70	01000110	11010001000
71	01000111	11001001000
72	01001000	11000101000
73	01001001	11000011000
74	01001010	10011001000
75	01001011	10010101000
76	01001100	10010011000
77	01001101	10001101000
78	01001110	10001011000
79	01001111	10000111000
80	01010000	10010100010
81	01010001	11010000100
82	01010010	11010000010
83	01010011	11001000100

Start Bit

Table 4-5 (Continued)

	Input Code	Constant Ratio Code
84	01010100	11001000010
85	01010101	11000100100
86	01010110	11000100010
87	01010111	11000010100
88	01011000	11000010010
89	01011001	11000001100
90	01011010	11000001010
91	01011011	11000000011
92	01011100	11000000110
93	01011101	10011000100
94	01011110	10011000010
95	01011111	10010100100
96	01100000	01010100010
97	01100001	10110000100
98	01100010	10110000010
99	01100011	10101000100
100	01100100	10101000010
101	01100101	10100100100
102	01100110	10100100010
103	01100111	10100010100
104	01101000	10100010010
105	01101001	10100001100
106	01101010	10100001010
107	01101011	10100000011
108	01101100	10100000110
109	01101101	01011000100
110	01101110	01011000010
111	01101111	01010100100

Start Bit

Table 4-6. 8-Bit Start-Stop

	Input Code	Constant Ratio Code
0	00000000	00011011000
1	00000001	00000010111
2	00000010	00000011011
3	00000011	00000011101
4	00000100	00000011110
5	00000101	00000100111
6	00000110	00000101011
7	00000111	00000101101
8	00001000	00000101110
9	00001001	00000110011
10	00001010	00000110101
11	00001011	00000110110
12	00001100	00000111001
13	00001101	00000111010
14	00001110	00000111100
15	00001111	00001000111
16	00010000	00001001011
17	00010001	00011100001
18	00010010	00001001110
19	00010011	00001010011
20	00010100	00001010101
21	00010101	00001010110
22	00010110	00001011001
23	00010111	00001011010
24	00011000	00001011100
25	00011001	00001100011
26	00011010	00001100101
27	00011011	00001100110

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
28	00011100	00001101001
29	00011101	00001101010
30	00011110	00001101100
31	00011111	00001001101
32	00100000	00001110001
33	00100001	00001110010
34	00100010	00001110100
35	00100011	00001111000
36	00100100	00010000111
37	00100101	00010001011
38	00100110	00010001101
39	00100111	00010001110
40	00101000	00010010011
41	00101001	00010010101
42	00101010	00010010110
43	00101011	00010011001
44	00101100	00010011010
45	00101101	00010011100
46	00101110	00010100011
47	00101111	00010100101
48	00110000	00010101001
49	00110001	00010101010
50	00110010	00010101100
51	00110011	00010110001
52	00110011	00010110001
53	00110101	00010110100
54	00110110	00010111000
55	00110111	00011000011

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
56	00111000	00011000101
57	00111001	00011000110
58	00111010	00011001001
59	00111011	00011001010
60	00111100	00011001100
61	00111101	00011010001
62	00111110	00011010010
63	00111111	00011010100
64	01000000	11100000100
65	01000001	11100000010
66	01000010	11010100000
67	01000011	11011000000
68	01000100	10011100000
69	01000101	10000000111
70	01000110	11010001000
71	01000111	11001001000
72	01001000	11000101000
73	01001001	11000011000
74	01001010	10011001000
75	01001011	10010101000
76	01001100	10010011000
77	01001101	10001101000
78	01001110	10001011000
79	01001111	10000111000
80	01010000	10010100010
81	01010001	11010000100
82	01010010	11010000010
83	01010011	11001000100

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
84	01010100	11001000010
85	01010101	11000100100
86	01010110	11000100010
87	01010111	11000010100
88	01011000	11000010010
89	01011001	11000001100
90	01011010	11000001010
91	01011011	11000000011
92	01011100	11000000110
93	01011101	10011000100
94	01011110	10011000010
95	01011111	10010100100
96	01100000	01010100010
97	01100001	10110000100
98	01100010	10110000010
99	01100011	10101000100
100	01100100	10101000010
101	01100101	10100100100
102	01100110	10100100010
103	01100111	10100010100
104	01101000	10100010010
105	01101001	10100001100
106	01101010	10100001010
107	01101011	10100000011
108	01101100	10100000110
109	01101101	01011000100
110	01101110	01011000010
111	01101111	01010100100

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
112	01110000	00110100010
113	01110001	01110000100
114	01110010	01110000010
115	01110011	01101000100
116	01110100	01101000010
117	01110101	01100100100
118	01110110	01100100010
119	01110111	01100010100
120	01111000	01100010010
121	01111001	01100001100
122	01111010	01100001010
123	01111011	01100000011
124	01111100	01100000110
125	01111101	00111000100
126	01111110	00111000010
127	01111111	00110100100
128	10000000	10010010010
129	10000001	10010010100
130	10000010	10010001010
131	10000011	10010001100
132	10000100	10010000110
133	10000101	10010000011
134	10000110	10001100010
135	10000111	10001100100
136	10001000	10001010010
137	10001001	10001010100
138	10001010	10001001010
139	10001011	10001001100

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
140	10001100	10001000110
141	10001101	10001000011
142	10001110	10000110010
143	10001111	10000110100
144	10010000	01010010010
145	10010001	01010010100
146	10010010	01010001010
147	10010011	01010001100
148	10010100	01010000110
149	10010101	01010000011
150	10010110	01011100010
151	10010111	01001100100
152	10011000	01001010010
153	10011001	01001010100
154	10011010	01001001010
155	10011011	01001001100
156	10011100	01001000110
157	10011101	01001000011
158	10011110	01000110010
159	10011111	01000110100
160	10100000	00110010010
161	10100001	00110010100
162	10100010	00110001010
163	10100011	00110001100
164	10100100	00110000110
165	10100101	00110000011
166	10100110	00101100010
167	10100111	00101100100

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
168	10101000	00101010010
169	10101001	00101010100
170	10101010	00101001010
171	10101011	00101001100
172	10101100	00101000110
173	10101101	00101000011
174	10101110	00100110010
175	10101111	00100110100
176	10110000	10000101010
177	10110001	10000101100
178	10110010	10000100110
179	10110011	10000100011
180	10110100	10000011010
181	10110101	10000011100
182	10110110	10000010110
183	10110111	10000010011
184	10111000	10000001110
185	10111001	10000001011
186	10111010	11010010000
187	10111011	11001010000
188	10111100	11000110000
189	10111101	10011010000
190	10111110	10010110000
191	10111111	11011000000
192	11000000	01000101010
193	11000001	01000101100
194	11000010	01000100110
195	11000011	01000100011

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
196	11000100	01000011010
197	11000101	01000011100
198	11000110	01000010110
199	11000111	01000010011
200	11001000	01000001110
201	11001001	01000001011
202	11001010	10110010000
203	11001011	10101010000
204	11001100	10100110000
205	11001101	01011010000
206	11001110	01010110000
207	11001111	10111000000
208	11010000	00100101010
209	11010001	00100101100
210	11010010	00100100110
211	11010011	00100100011
212	11010100	00100011010
213	11010101	00100011100
214	11010110	00100010110
215	11010111	00100010011
216	11011000	00100001110
217	11011001	00100001011
218	11011010	01110010000
219	11011011	01110101000
220	11011100	01100110000
221	11011101	00111010000
222	11011110	00110110000
223	11011111	01111000000

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
224	11100000	11100010000
225	11100001	11100100000
226	11100010	10110100000
227	11100011	10101100000
228	11100100	01011100000
229	11100101	01000000111
230	11100110	10110001000
231	11100111	10101001000
232	11101000	10100101000
233	11101001	10100011000
234	11101010	01011001000
235	11101011	01010101000
236	11101100	01010011000
237	11101101	01001101000
238	11101110	01001011000
239	11101111	01000111000
240	11110000	11101000000
241	11110001	11100001000
242	11110010	01110100000
243	11110011	01101100000
244	11110100	00111100000
245	11110101	00100000111
246	11110110	01110001000
247	11110111	01101001000
248	11111000	01100101000
249	11111001	01100011000
250	11111010	00111001000
251	11111011	00110101000

Table 4-6. (Continued)

	Input Code	Constant Ratio Code
252	11111100	00110011000
253	11111101	00101101000
254	11111110	00101011000
255	11111111	00100111000

Table 4-7.

Unused Constant Ratio Codes

Mode	Number Input Code	Number Supervisor Codes	Total Codes	Constant Ratio Code Length	Total Available Const. Ratio Comb.	Total No. Un-Used Combin.	Method of Detecting Un-Used Codes
Bit Stream	64	6	70	8	70	--	
5 Bit S-S	32	6	38	8	70	32	First 3 bits of output code must be (LOW) for valid combination; the third bit will form start bit
6 Bit S-S	64	6	70	11	330	260	In 11 bit constant ratio codes 68 combinations are always declared un-used in addition for 6 bit S-S; first bit of output code must be HIGH and the second bit must be LOW for valid combination; the second bit will form start bit
7 Bit S-S	128	6	134	11	330	196	First bit of output code must be (LOW) for valid combination; this bit will form start bit.
8 Bit S-S	256	6	262	11	330	68	All 8 bit line codes are valid; start bit is generated externally from decoder.

Table 4-8. 11-Bit Constant Ratio Unused Codes.

1 -64 -	001xxxxxx01 010xxxxxx01 011xxxxxx01 100xxxxxx01 101xxxxxx01 110xxxxxx01 111xxxxxx01	If 11 Bit Constant Ratio Code ends with 01 then any of the first three bits must not be (HIGH); if so, combination is invalid. This invalidates 64 code combinations.
65 -	00011110000	Considered invalid by Receiver
66 -	00101110000	
67 -	01001110000	
68 -	10001110000	

II - SYSTEM OPERATION

4-3. INITIALIZATION. - The initialization sequence is illustrated in Figure A -53, which shows the initialization of a single AN/FYC-12 from the time that power is turned on or the initialization switch (S7) is operated. Both ends of the communications link using the [1]Digital Data Set must be initialized before normal communications can commence. The signal INIT 1 is generated 400 milliseconds after power turn on or the initialization switch is operated. It has a duration of 50 microseconds and starts the initialization sequence that is illustrated in Figure A -53.

a. Transmitter Logic. - The transmitter logic may require 15 bit times before all the logical counters and flip-flops are initialized, when the signal INIT 3 goes INACTIVE (HIGH). During this time, the transmitter send line is held HIGH to prevent any spurious data from being transmitted. The transmitter memory is then initialized by loading every used address with the Inhibit Activate supervisory character; the supervisory character is also transmitted to the distant receiver at this time and may require from eight to 68 character times to complete the operation, depending upon the memory length selected. When the memory is completely initialized, the signal INIT goes INACTIVE (HIGH) and allows the transmitter to respond to any flags that the receiver may have raised during the initialization sequence.

b. Receiver Logic. - The receiver logic is initialized immediately by the signal INIT 1 and can receive constant ratio codes immediately after power turn -on. The receiver ARQ FLG signal is not initialized but will be set active after receiving the first character. (The first character is declared invalid because it is improbable that both ends of the communications link will be brought on line at the same instant and in synchronization).

4-4. DATA FLOW. - The data flow for a communication system that uses Digital Data Set AN/FYC-12 for error detecting and correcting is shown in Figure 1-2. At each end of the system is a data source to send data, and a data sink to receive data, shown as part of the digital data terminal in the diagram. The data terminal also generates a system clock at twice the data baud rate, and has provision for communication system controls and indicators. The Digital Data Set transmits and receives utilizing a standard (MIL-STD 188C) low level dc signal interface, and for long distance communica-

tions a data modern is required to modulate the signals, with a carrier, This modem also derives the synchronous receiver clock signal at twice the data rate; the clock is phased so that its fall occurs at the center of each data bit. In normal operation the system is full duplex with the data flow in both directions at the same time. The data rates (baud) must be similar (±2%) in both directions but no special phase relationship is required between the two transmitter clock signals.

a. Transmitter Step Clock. - The The flow of data is controlled by the transmitter step clock signal and in all start-stop modes one complete character is processed for every step clock signal (the step clock has a duration of two transmitter bit times). Hence the AN/FYC-12 outputs a start signal (step clock) when it requires a new character from the data source. In bit stream mode the transmitter step clock is six complete cycles of the transmitter clock for each data character required and the data source must output one bit for each cycle of the step clock. The AN/FYC-12 transmitter has full control over the data source,, which can only output data when commanded to do so by the transmitter. This control is essential for the proper operation of the complete system. The data source sends each character as a serial sequence of data bits, and the transmitter converts each character into a parallel combination of eight bits. (If the terminal code has been less than eight bits, the transmitter sets the spare bits to definite states.) The transmitter can also generate supervisory control characters that are used to control the flow of data in the complete system and adds them to the normal data characters, Each character is remembered in the transmitter memory (all the data characters have eight bits but the supervisory control characters have nine). They are encoded into a constant ratio code eight bits wide for bit stream and 5-bit start-stop input formats and eleven bits wide for 6-, 7- and 8- bit start-stop formats. The transmitter can also generate supervisory control characters after the memory and encoder, to enable the distant receiver to synchronize to the constant ratio code that is being transmitted. During the next character time the 8-bit or 11-bit constant ratio code is serially transmitted to the distant receiver. The transmitter memory is adjustable from eight to 64 characters (increments of four characters). The character is transmitted immediately (next character) but the transmitter can remember the last 64 characters that were transmitted and, if requested, may retransmit them from its memory.

b. Receiver. - The AN/FYC-12 receiver receives the 8-bit or 11-bit constant ratio codes from the transmitter as a serial sequence of bits and hence must be synchronized so as to know where each new constant ratio code begins with respect to time. This is achieved with a resynchronizing sequence known as a SYNC CYCLE, fully described in paragraph 4-6. The receiver is considered synchronized for the present data flow description. The receiver converts the 8 bit or 11-bit constant ratio codes into a parallel combination of eight or 11 bits that make up each data character. The data

l's are counted to verify that each constant ratio code has four. If not, a nonconstant ratio code error signal is generated. The receiver also checks the eight or eleven bits of the constant ratio code for the control supervisory characters, which it inhibits from the data sink and takes the required action.

c. Number of Constant Ratio Codes. - The number of code combinations that can be transmitted depends upon the input format. Many of the available constant ratio codes are unused in some input formats (see Table 4-7), so the receiver checks that the constant ratio code received is used in the selected input format and if not, an unused constant ratio code error signal is generated. The nonconstant ratio code error signal and the unused constant ratio code error signal, together with the supervisory control character, ARQ cause the receiver to request a data retransmission and the system enters an ARQ sequence known as an ARQ CYCLE (described in paragraph 4-5). If the received constant ratio code is valid, and not a supervisory control character, the receiver decodes it into the original data terminal code; during the next character time it sends this code serially--with the correct start and stop bits (start-stop modes only)--to the data sink. The receiver also generates a step clock signal, which may control the data sink. In all start-stop modes it is a single pulse that marks the start bit of each new character; but in bit stream it is six cycles of the receiver clock that mark each separate bit of the six bit, bit stream character.

d. Time for Each Character. - The constant ratio code bit time is the same as the terminal code bit time and, because the constant ratio code is at least two bits longer than the terminal code, the data terminal is idle for at least two bit times in every character.

4-5. ARQ CYCLE. - The purpose of an ARQ cycle is to retransmit a sequence of data from the transmitter memory when an error is detected. The sequence is illustrated in Figure A-54. This shows a data communication link between a local AN/FYC-12 (transmitter at the top and receiver at the bottom) and a distant AN/FYC-12 (CENTER). The local transmitter is sending the alphabet (A-Z) to the distant receiver and the distant transmitter is sending numbers (1-26) to the local receiver. Each character is requested from the data source, memorized, encoded, transmitted, received, validated decoded and sent to the data sink. Referring to the diagram (Figure A-54), when the distant receiver receives the letter H, it detects an error in transmission, raises the receiver ARQ flag to the distant transmitter, and inhibits the erroneous character (H) from being sent to the data sink, It also starts the ARQ character counter, which counts one transmitter memory length and inhibits all data to the data sink during this count. It is important for proper system generation that the selected memory length at the local and distant end be the same. In the sequence illustrated in Figure A-54 position 3 is selected, giving a memory length of 16 characters.

a. The Distant Transmitter. - The distant transmitter recognizes the receiver ARQ flag at the end of a character time, marks the memory address of this character with an ARQ marker bit before transmitting the character and entering the ARQ sequence. The transmitter inhibits the step clock so that new characters are not requested from the data source, and generates two sequential ARQ supervisory control characters, which are stored in the memory and transmitted in the usual way. The transmitter also clears the receiver ARQ flag at this time and the receiver is not able to raise it again until the end of its ARQ sequence. After transmitting the two ARQ supervisory control characters, the transmitter's memory write command is inhibited, so that as the memory is incremented at the end of each character the transmitter encodes and transmits the character that was originally saved at each memory address, starting two characters after the ARQ marker bit. Again referring to Figure A-54, the first character after the two ARQ's is an IDLE supervisor character followed by another IDLE and the number 1 through 12. (The reason for the IDLE supervisors is that the transmitter was idle before beginning to transmit the numbers 1-26.) After a propagation delay (four characters in the example) the local receiver receives the first ARQ supervisory control character and enters into its own ARQ sequence, raising its ARQ flag to the local transmitter and inhibiting the flow of data to the local data sink for one memory length. In the illustration (Figure A-54) this occurs after receiving the number 12, the next character received being the ARQ supervisor followed by the second ARQ supervisor. This sets the TWO ARQ's RCVD flag enabling the receiver to leave the ARQ sequence after counting one memory length, if the error is not repeated.

b. The Local Transmitter. - The local transmitter recognizes the receiver ARQ flag at the end of a character time; it marks the memory address of this character with an ARQ marker bit before transmitting the character and entering the ARQ sequence. The transmitter inhibits the step clock so that new characters are not requested from the data source, and generates two sequential ARQ supervisory control characters, which are stored in the memory and transmitted in the usual way. The transmitter clears the receiver ARQ flag and continues to transmit from its memory. Again referring to Figure A-54 the last character transmitted before the ARQ flag is the letter Q, which is marked with an ARQ marker bit. The local transmitter transmits the two ARQ's followed by the letters D through Q, at this point both the distant and local ends of the communication system have entered the ARQ sequence and are retransmitting data characters from memory, the data step clocks are inhibited, and no new data is being processed at either end of the system.

C. The Distant Receiver. - The distant receiver, which initiated the ARQ sequence, receives the two ARQ supervisor, after another propagation delay (four characters in the example) but it is not permitted to raise its ARQ flag because it is still in an active ARQ sequence. But the two sequential ARQ's received will set the TWO ARQ's RCVD flag enabling the receiver to leave

the ARQ sequence at the end of one memory length, if the error is not repeated. The receiver ARQ character counter has been counting the number of characters received; after one memory length (16 characters in the example), it enables the receiver to examine the next character. As shown in the diagram (Figure A-54) this character is the one that caused the original error- the letter H. The receiver validates and, if correct, the distant receiver leaves the ARQ sequence provided that two sequential ARQ's have been received during the ARQ sequence. If the character is still invalid, or if two sequential ARQ's have not been received, the receiver again raises the ARQ flag; and the ARQ sequence repeats. In the diagram the character is considered valid and the distant receiver sends the character to the data sink and leaves the ARQ sequence.

d. Leaving the ARQ Sequence. - The distant transmitter has been transmitting data characters from memory; after one memory length the ARQ marker bit is read and, provided that the receiver has not repeated the ARQ flag, the distant transmitter also leaves the ARQ sequence enabling its step clock and requesting a new data character from the distant data source. In the same manner the local receiver also counts out one memory length and validates the next character; if it is good, and if two ARQ's have been received, it leaves the ARQ sequence, sending the character to the local data sink. In the diagram (Figure A-54) this character is the number 13, which is considered valid and sent to the data sink. The local transmitter has also been transmitting data character from memory and, after one memory length, it detects the ARQ marker bit; if the local receiver has not repeated the ARQ flag, it also leaves the ARQ sequence, enabling its step clock to request a new data character from the local data source. In the diagram (Figure A -54) the local receiver detects an error on the number 14. As an example of the ARQ sequence the reader should determine the sequence of the ARQ through the local and distant ends of the system until normal transmission is resumed

e. ARQ Indicators. - Two front panel indicators indicate the status of an ARQ cycle; the receiver illuminates the mutilated character indicator (MC) if a nonconstant ratio or unused code is received. This indicator is on for the complete ARQ sequence when the receiver is inhibiting data to the data sink. It is extinguished when the receiver next examines a character at the end of the ARQ sequence. With a constant ARQ this indicator flashes off for one character during each ARQ sequence while the receiver tries to validate a character. The ARQ indicator is illuminated by the transmitter after responding to an ARQ flag set by the receiver. It remains illuminated until the system leaves the ARQ cycle. Thus at the AN/FYC-12 that detected the error the MC and ARQ indicators are illuminated; but the other AN/FYC-12 will have only the ARQ indicator illuminated.

4-6. SYNC CYCLE. - The purpose of a SYNC cycle is to retime the receiver last bit to be synchronous with the incoming data; a complete cycle is illus-

trated in Figure A-55. The communication system in this illustration is the same as for an ARQ cycle in Figure A-54; it must be in an ARQ cycle to enable the operator at either end of the system to initiate a resynchronization sequence, which is always a manual operation. Referring to Figure A-55 the local transmitter is sending the alphabet (A-Z) to the distant receiver, and the distant transmitter is sending numbers (l-23) to the local receiver. When the distant receiver receives the letter H, a change of propagation time results in a loss of synchronization. The receiver invalidates the character and initiates an ARQ cycle. The data being received by the distant receiver is constantly mutilated due to the error in synchronization and the ARQ cycle repeats continually. Both ends of the communication system are closed down, with the distant and local transmitters continually repeating the last data sequence from memory.

a. Initiation of the Resynchronization Sequence. - The operator at the local end now initiates a resynchronization sequence by operating the SYNC switch (S3) on the front panel, or using the remote control line. The local transmitter recognizes this at the end of a character time and marks the memory address with a sync cycle marker bit, but does not change any data character in the memory. The local transmitter enters a resynchronization sequence, inhibits the data characters being transmitted from memory, and transmits one memory length of supervisory control characters, but does not store them or change the memorized data characters in any way. The first supervisory character transmitted is SYNC A, followed by SYNC B; the memory length is completed with Inhibit ACTIVATE or DEACTIVATE depending upon the position of the front panel INHIBIT switch (S5) or its remote control line. The supervisory characters SYNC A followed by SYNC B transmit a unique sequence of eight sequential l's followed by four or seven O's and can be recognized by the receiver at any bit time.

b. The Distant Receiver. - The distant receiver receives the two supervisory characters SYNC A and SYNC B after a propagation delay and recognizes the sequence at any bit time, then forces the supervisory character SYNC B to be correctly synchronized by generating a new last bit time. The receiver generates a sync flag No. 1 to the distant transmitter when a resynchronization occurs and a sync flag No. 2 if an Inhibit ACTIVATE or Inhibit DEACTIVATE supervisory character is correctly received after resynchronization indicating that correct synchronization has been achieved. The added receiver last bit generated by a resynchronization sequence may cause an error in the ARQ character counter (this counter counts the receiver last bit times to determine the total number of characters received during an ARQ cycle). If, after resynchronization, the new last bit occurs during the first half of the old character, it is assumed to be caused by a delayed character and is not counted by the ARQ character counter; but if the new last bit time occurs during the last half of the old character it is assumed to be caused by an advanced character and is counted. The ARQ character counter

can keep count of the number of characters received providing the synchronization does not change by more than ± half a character time. The receiver also starts a character counter that holds the system in the ARQ sequence for at least two memory lengths after resynchronization occurs.

c. The Distant Transmitter. - The distant transmitter responds to the receiver sync flag No. 1 at the end of a character time and marks the memory address with a sync cycle marker bit; then the distant transmitter enters the sync sequence and transmits the same resynchronization data sequence as the local transmitter did but does not change any data characters in its memory. Referring to the diagram (Figure A-55) the local transmitter responds to the operator's request for resynchronization after the letter H and marks it with a sync marker bit before transmitting the resynchronization sequence, which the distant receiver receives after a propagation delay. The distant receiver resynchronizes and generates sync flag signal No. 1. If the inhibit character is correctly received during the next character Lime, it also generates sync flag signal No. 2. The distant transmitter responds to sync flag No. 1 after the character No. 2 and marks it with a sync marker bit before, also transmitting the resynchronization sequence to the local receiver, The local receiver resynchronizes and sets the flags, but because the local transmitter is already transmitting a resynchronization sequence sync flag No. 1 cannot generate another one. At this time the receivers at both ends of the system have been resynchronized and--if they have correctly received either of the inhibit supervisory characters after resynchronization--all the sync flags are set; the transmitters are transmitting the selected inhibit supervisory character. When the transmitter has completed one memory length, the sync marker bit is repeated and the transmitter checks to ensure that both the receiver sync flags No. 1 and No. 2 have been generated and that the transmitter is transmitting inhibit supervisory characters. If so, it resets both the receivers sync flags and detects the sync marker bit from the memory before returning to the original ARQ cycle and transmitting data characters from memory. If not, it repeats the resynchronization sequence. In the diagram (Figure A-55) the local transmitter returns to the letter M and the distant transmitter to the number 3; the ARQ cycle is held by the receivers for at least two memory lengths after resynchronization by the receiver sync character counter. When the distant receiver receives the letter H after two ARQ cycles, it validates it and sends it to the data sink, leaving the ARQ cycle. The distant transmitter, after detecting the ARQ marker bit on the number 12, leaves the ARQ cycle, requesting the next character from the data source. The local receiver validates the number 13 and sends it to the data sink; the local transmitter leaves the ARQ cycle after the letter Q, requesting a new character from the local data source. The same sequence would have occurred if the operator at the distant transmitter had initiated the resynchronization sequence.

d. Sync Cycle Indicator. - The sync cycle indicator is illuminated by the transmitter after entering the resynchronization sequence bit is held illuminated by the receiver until it also leaves the resynchronization sequence.

4-7. INHIBIT OPERATION. - The local operator can control the distant transmitter with the INHIBIT control on the front panel of the AN/FYC-12 (S5) or its remote control line. When the INHIBIT control is changed from INHIBIT DEACTIVATE to INHIBIT ACTIVATE, the transmitter halts the data source for one character and transmits the Inhibit ACTIVATE supervisory character. When the control is changed from INHIBIT ACTIVATE to INHIBIT DEACTIVATE, the Inhibit DEACTIVATE supervisory character is transmitted for one character. The front panel indicator INHIBIT REQ is illuminated when the Inhibit ACTIVATE supervisory character is transmitted, and extinguished when the Inhibit DEACTIVATE supervisory character is transmitted. The distant receiver responds to the Inhibit ACTIVATE supervisory character by raising a flag to the distant transmitter, and to the Inhibit DEACTIVATE supervisory character by lowering the same flag. The distant transmitter responds to the receiver inhibit flag at the end of the next character one of two ways--depending upon the Inhibit Strap option. In option A the indicator INHIBIT RCVD is illuminated and the step clock halted; the transmitter continues to transmit the inhibit supervisor selected on the front panel switches or remote line. In option B only the indicator INHIBIT RCVD is illuminated. When the receiver lowers the inhibit flag, the transmitter returns to normal data flow at the end of the active character time, extinguishing the indicator INHIBIT RCVD.

III - UNIT OPERATION

4-8. INITIALIZATION. - Initialization of the AN/FYC-12 consists of setting up the starting conditions for the memory, counters and flip-flops so that it can be synchronized with a distant system and then transmit and receive data. At power turn -on, or when the initialization switch is operated, the dc-dc converter (A2A17) generates an initialization signal INIT 1, which is a positive pulse 50 microseconds long; it starts the initialization sequence (Figure A-53).

a. Transmitter Logic. - The transmitter controls the initialization sequence with the initialize logic (XMTR 13), which inverts the initialization signal INIT 1 into the signal INIT and is active LOW for 50 microseconds beginning 400 milliseconds after power is applied or the initialization switch is operated. This block also generates the initialization signals INIT 3, which remains active (LOW) until the transmitter data source enable logic has been initialized (this requires 15 transmitter bit times), and INIT 2, which remains active (LOW) until the transmitter memory has been initialized with Inhibit ACTIVATE supervisory characters (this may require 68

characters times). The signal INIT 1 initializes the following logical components:

1. Sample Enable (XMTR 10)	A2A1	U3 (Figure A-18) U14A (Figure A-6)
2. Initialize Logic (XMTR 13)	A2A2	U2A, U2B (Figure A -14)
3. XMTR Bit Counter (XMTR 15)	A2A2	U6 (Figure A-21)
4. XMTR Last Bit Counter (XMTR 16)	A2A2	U3 (Figure A-18)
5. Memory Address Counter (XMTR 38)	A2A6	U14 (Figure A-19) - U6A, U6B (Figure A -16) U12B (Figure A-14)

The transmitter step clock signal X CLK ST and the sample start signal X ST SMPL EN are disabled by the control signal X IN DA INH being set true (LOW) by the inhibit received signal, X DA INH RCVD, which is held true (LOW) by the Initialization signal INIT 2. The inhibit select signal LNH SWITCH A/D is set HIGH by the inhibit request control (XMTR 23); the inhibit generate signal LNH GEN is set LOW by the inhibit received control (XMTR 22); the memorized supervisor control (XMTR 39) logic selects the supervisor mode when initialized by the signal INIT 2 for the duration of the initialization sequence. The transmitter ARQ and SYNC cycle control logic (XMTR 25 and XMTR 27) are also held reset and unable to respond to the receiver flags by the initialize signal INIT 2. The sample enable logic (XMTR 10) is reset by the signal INIT and requires 15 clock pulses for the counter A2A1U3 to reach maximum count when the carry output (pin 15) goes HIGH; the counter is clocked by the signal X SMPL CTR CLK, which occurs once per transmitter bit time. (During normal data flow this occurs at the center of each data input bit; but during initialization it occurs at the same time as the signal X N CLK). On the sixteenth clock pulse to counter A2A1U3 the counter loads the contents of the inputs A, B, C and D with a number dependent upon the input format selected (See Table 4-9). NAND gate A2A1U1B is enabled so that the J input (Pin 1) of flip-flop A2A1U14A goes HIGH and is preset by the fall of the fast clock. This enables the memory write control (XMTR 24) to generate a memory write signal MEM WRITE A, after the timing signal X NL CLK. The Inhibit ACTIVATE supervisory character generated by XMTR 36 is written into the first memory address. The transmitter output signal SEND LIN has been held HIGH by the initialization signal INIT 3, which presets the timing flip-flop A2A5U7A in parallel-to-serial converter XMTR 33. After the first memory write pulse the initialization signal INIT 3

goes false (HIGH), which enables the transmitter to transmit the Inhibit ACTIVATE supervisory character during the next character time. The memory address counter is incremented by the timing signal X PL, CLK and another Inhibit ACTIVATE supervisory character is written into the second memory address and transmitted. This procedure is repeated for one memory length plus four characters, when the control signal MEM ADD MAX goes HIGH and sets the initialization signal INIT 2 false (HIGH). This completes the initialization sequence (every used memory address now contains the Inhibit ACTIVATE supervisory character, which is valid in all formats). The next character after the initialization sequence is always an Idle supervisor, At this time the transmitter is enabled to test any receiver flags that may have been raised during the transmitter initialization sequence. The Idle is generated in start-stop modes because the step clock signal X CLK ST is omitted for this character time; hence no start- bit can be detected. In bit stream the control signal INH GEN disables NAND gate A2A1U9A which prevents enable flip-flop A2A1U14A being reset and therefore an Idle supervisor is also generated. The signal INIT 2 initializes the following logical components :

1. Inhibit Request Control (XMTR 23)	A2A3 U13A, U18B (Figure A-17) U11B, U11C (Figure A-4)
2. Inhibit Received Control (XMTR 22)	A2A3 U1A, U8A, U8B (Figure A-14)
3. XMTR ARQ Cycle Control (XMTR 25)	A2A4 U5A, U5B, (Figure A-14) U11A, U11B, U18A, U10B (Figure A-16)
4. XMTR SYNC Cycle Control (XMTR 27)	A2A4 U4B, U9A (Figure A-14) U10A, U14A, U14B (Figure A-16)
5. Memorized Supervisor Control (XMTR 38)	A2A6 U12A (Figure A-14)

The signal INIT initializes the following logical components:

1. Parallel -To -Serial Converter (XMTR 33)	A2A5 U7A (Figure A-14)

b. Receiver Logic. - The receiver logic is all initialized by the initialization signal in and is able to receive constant ratio code data immediately. Due to the very low probability that the distant transmitter is placed on line at the same instant and in synchronization with the receiver, the first character received is mutilated and generates an ARQ flag to which the transmitter responds after completing it own initialization. The signal INLT 1 initializes the following logical components:

1. UN-SYNC A (RCVR 6)	A2A10	U4A, U21A (Figure A-14) U5B (Figure A-15)
2. RCVR Bit Counter (RCVR 5)	A2A10	UP6 (Figure A-18)
3. Clock Step Generator (RCVR 9)	A2A10	U4B (Figure A-14) U5A (Figure A-15)
4. Data Inhibit Control (RCVR 10)	A2A10	U13A, U13B (Figure A -16)
5. MC Indicator (RCVR 20)	A2A11	U20A (Figure A-15)
6. Two ARQ's Detector (RCVR 22)	A2A11	U24B (Figure A -14)
7. ARQ Cycle Counter (RCVR 24)	A2A11	U3 (Figure A-19) U21A, U21B (Figure A -15)
8. SYNC Cycle Counter (RCVR 25)	A2A11	U1, U2 (Figure A -19) U18B (Figure A -15)
9. Inhibit Flag (RCVR 27)	A2A11	U13A (Figure A -15)
10. Sync Flag (RCVR 28)	A2A11	U12A, U12B (Figure A -15)
11. Sync Pattern Detector (RCVR 21)	A2A11	U8 (Figure A-18) U13B (Figure A -15)

The complete initialization sequence for the AN/FYC-12 is illustrated in Figure A -53.

4-9. DATA FLOW. - The transmitter requests the next character with a step clock signal X CLK ST L via a LOW level dc (MIL STD 188C) interface. In bit stream each step clock pulse requests one data bit.) The data source has

two transmitter bit times to respond with the first bit of the next character. In start-stop modes this is always a start bit (LOW) and is used by the transmitter to determine the center of each data bit. In bit stream however this is the first data bit and can be HIGH or LOW depending upon the data to be transmitted. Therefore, in the bit stream mode the center sampling for the incoming data must be manually adjusted. The incoming data bits and the station clock (which has a frequency twice the data rate) are received from the data source via a LOW level dc interface (MIL STD 188C) and are converted into transistor-transistor logic (TTL) levels by the line receivers (XMTR 1) and (XMTR 2). The TTL signals X IN DA and X CLK are the incoming data and timing signals for the transmitter. Two remote control signals are also received from the data source by low-level dc interface, which initiate a SYNC CYCLE (SYNC INT L) or halt. the distant data source (LOCAL END INH L); they are converted into TTL levels by the line receivers XMTR 3 and XMTR 4, which generate the control signals SYNC INT and LOCAL INH.

a. Incoming Data. - The incoming data characters are received from the data source bit by bit and the serial-to-parallel converter (XMTR 35) converts each character into a parallel combination (in bit stream each character has six data bits). The bits are clocked into the serial-to-parallel converter at the center of each bit time by the timing signal X SP CLK and generate an 8-bit parallel code (In S-bit start-stop and bit stream the first two bits are always forced LOW; in 6-bit start-stop the first bit is always forced HIGH, and in 8-bit, 6-bit, 7-bit start-stop the start bit (LOW) is included as part of the character terminal code).

b. Transmitted Supervisory Control Characters. - At this point the data flow can be interrupted and four supervisory control characters generated using a ninth bit to identify them. The control characters are:

1. Idle - If the data source does not respond to the step clock within two bit times in start-s top modes, an Idle supervisor character is transmitted.

2. Inhibit Activate - If the operator requests the distant data source to close down with the inhibit switch, normal data is interrupted for one character time and the Inhibit ACTIVATE supervisory character is transmitted instead.

3. Inhibit Deactivate - If the operator requests data from the distant source with the inhibit switch, normal data is interrupted for one character time and the Inhibit DEACTIVE supervisory character transmitted instead.

4. ARQ - If the receiver detects an error in transmission or receives the ARQ supervisory character, it requests a re-transmission of previous data from the memory. This retransmission is always preceeded by two ARQ supervisory characters.

c. Distant Transmitter Inhibit. - When the data source has been closed down by the distant station, the transmitter constantly transmits the Inhibit DEACTIVATE or Inhibit ACTIVATE supervisory character depending upon the position of the INHIBIT switch or its remote control line. To generate the control supervisory characters the data output of the serial-to-parallel converter is inhibited by the Memorized Supervisor Data Inhibit (XMTR 36) logic and the code for the required supervisory character generated by the Memorized Supervisor Generator (XMTR 37). The operation is controlled by the Memorized Supervisor Control (XMTR 38) logic.

d. System Memory. - The nine parallel data bits are stored by the Memory B (XMTR 41), which has 64 9-bit locations that are sequentially addressed by the Memory Address Counter (XMTR 39). The actual number of used locations (Memory Length) is selected by the memory length switch--between 8 and 64 in four-step increments. The memory address counter is cyclic so that after the last used location has been filled, the next character replaces the character stored earlier in the first location. An extra parity bit is added to the data stored in memory and this bit is used to check the memory, a front panel indicator PARITY FAIL is illuminated when a memory error is detected. It can be manually reset with the PARITY RESET switch.

d. Parallel-To-Serial Conversion. - After a memory write signal $\overline{\text{MEM WRITE B}}$, which occurs only during normal data flow, after the last bit of the character code is shifted into the serial-to-parallel converter; the memory B (XMTR 41) output is identical to the input. During normal data flow the data character codes are read from the memory at the time they are stored.

f. Resynchronization. - During a resynchronization sequence the memory output is inhibited by the Sync Cycle Data Inhibit (XMTR 29) logic. This inhibits the memory output so that the Sync Cycle Activate or Deactivate Generator (XMTR 30) can generate the Inhibit ACTIVATE or Inhibit DEACTIVATE supervisory character without changing in any way the characters stored in memory B. The eight terminal code bits form the address for the Constant Ratio Code Encoder (XMTR 31) which encodes the terminal codes into 8-bit or 11-bit constant ratio codes. The ninth bit (supervisory marker bit). is used to change four of the generated constant ratio codes into the control supervisory character constant ratio codes by interchanging two bit positions. The output of the constant ratio code encoder is also modified during the first two characters of a resynchronization sequence by the Sync A and

Sync B Generator (XMTR 32) to generate the two supervisory characters SYNC A and SYNC B. These are always generated together and form a unique sequence of eight l's followed by four or seven 0's that can be recognized by the receiver at any bit time for resynchronization purposes.

g. Data Transmission. - For transmission the constant ratio code is loaded into the Parallel-To-Serial Converter by the timing signal X PS CLK at last bit time; this occurs 3 microseconds after the memory write signal MEM WRITE B giving enough setting time for RAM's and ROM's, The 8 -bit or 11-bit constant ratio code is transmitted bit by bit; at the same time, the next character is being received bit by bit from the data source. The transmitted constant ratio code is phased with the station clock; it is a continuous bit stream, all characters having four 1's and four or seven 0's and no blanks. The TTL data output signal SEND LIN is converted to a bipolar low level dc interface signal (MIL STD 188C) with voltage and current limiting by the Line Driver (XMTR 44) logic, which generates the transmitter data output signal SND LIN L.

h. Transmitter Indicators. - Three transmitter status indicator signals are also transmitted by LOW level dc interface signals to the data terminal. They indicate that the transmitter is in an ARQ cycle, (ARQ IND L) or a SYNC cycle (SYNC IND L), or that the distant end has transmitted the Inhibit ACTIVATE supervisory character and closed down or requested close down of the local data source (R DIST END INH).

i. Data Reception. - The receiver receives constant ratio codes via a LOW level dc interface and the Line Receiver (RCVR 1.) converts the bipolar signals into TTL compatible constant ratio signals. The receiving modem (not part of the AN/FYC-12) also generates a timing signal that has twice the rate of the incoming data and is phased so that the fall of the timing signal is at the center of each constant ratio data bit. This signal is known as the receiver clock R CLK and is converted to a TTL compatible signal by the Line Receiver (RCVR 2) l

j. Receiver Test Mode. - The data flow at the input of the receiver can be interrupted by placing the system in the Test Mode. The Test Normal Mode (RCVR 3) logic functions like a switch that in the normal mode accepts incoming data and a derived timing signal from the distant transmitter; but in Test Mode it accepts the timing and output constant ratio codes from the local transmitter. The sys tern is also forced into an ARQ cycle by the Test Unsync A (RCVR 6) logic that forces the system out of synchronization when the test mode is selected. When the test mode is selected, the line drivers and line receivers are not used, hence the test mode does not test any of the line interface logic on card assembly A2A8. The test mode enables the operator to test the local end of the system for data flow, resynchronization and ARQ operation, and greatly assists in troubleshooting.

k. Normal Data Flow. - Returning to the normal mode, the incoming constant ratio codes are retimed by the Input Data Timing (RCVR 12) logic which examines the incoming data bits at the center of each bit time using the timing signal R CLK to clock the flip-flop A2A9U4A. The receiver is receiving the incoming constant ratio code one bit at a time and the Serial-To-Parallel Converter (RCVR 14) converts the incoming data into an 8- or 11-bit parallel constant ratio code. If the receiver is correctly synchronized, the timing signal R BIT LAST is true (LOW) during the last bit time of every constant ratio code received and hence may signal that a complete character has been received. At the same time that each constant ratio code is being converted into a parallel combination, the number of l's is being ascertained by the Mutilated Character Detector (RCVR 13). If at the end of each character--when R BIT LAST is true (LOW)--four l's have not been received, a mutilated character is signalled by the control signal NCR RCVD. The serial-to-parallel converter is clocked by the timing signal R N1 CLK, which occurs at least 3 microseconds after the fall of the receiver clock R CLK.

1. Unused Constant Ratio Codes. - The constant ratio code format transmitted has many redundant codes and the receiver has to determine if the constant ratio code that has been received is used in the selected format, In the 11-bit constant ratio codes 68 codes are never used; these are decoded by the Unused Code Detector (RCVR 16) using inverters A2A9U15D, U15E, U15F, U15A,Ul8D,U18E,U18F (Figure A-1), NAND gates A2A9 U17 (Figure A-8), U21A (Figure A-4), U20A (Figure A-2) and NOR gates A2A9 U19C (Figure A-4) U20B (Figure A -2). This block is enabled only when 11-bit constant ratio codes are being received by the control signal CODE 11 BIT. The remaining unused constant ratio combinations are detected by testing the format of the decoded terminal code. The transmitter includes the start bit (always LOW) in 5-,6-, and 7-bit start-stop terminal modes. In 5-bit start-stop the first two bits are set LOW and in 6-bit start-stop the first bit is set HIGH. Inverters A2A9U13A, U13B, U18B (Figure A-1) and NOR gates A2A9U21C (Figure A-4), U14A (Figure A-2) test the decoded constant ratio codes for these formats and are enabled in the different operating terminal modes by NAND gates A2A9 U14C, U14D, U14B (Figure A-2) and the control signals 7-BIT S-S, 6-BIT S-S, S-BIT S-S. All the unused output signals in the different terminal modes are logically OR'ed with the negative logic NOR gate A2A9U7A. The six supervisory control characters cannot be decoded into the correct terminal code format and therefore are declared unused. To prevent this the six supervisory characters are logically OR'ed together; if any one is received it disables the unused output signal UNUSED RCVD with NAND gate A2A9U24C (Figure A-2). A complete constant ratio code must be on the output lines of the serial parallel converter to enable unused codes to be detected; hence the signal UNUSED RCVD is only valid during the received last bit time.

m. Invalid Constant Ratio Codes. - The signals NCR RCVD (nonconstant ratio) and UNUSED RCVD (unused constant ratio) are logically OR'ed to generate a mutilated character signal, which closes down the receiver data sink, starts a character counter and requests a retransmission of the mutilated data, This is called an ARQ cycle; it is described in paragraph 4-10.

n. Received Supervisory Control Characters. - The six supervisory control characters are also decoded from the parallel constant ratio codes. The supervisory characters IDLE, Inhibit ACTIVATE, Inhibit DEACTIVATE, and ARQ must be decoded at last bit time. CODE BIT 7 for all four characters is HIGH also if a constant ratio code of four l's is received; the control signal NCR RCVD is false (HIGH). These two signals are logically AND'ed using the gates A2A9U24A, U24B, (Figure A -2) so that the output (Pin 11) of gate U24B is HIGH if, CODE BIT 7 is HIGH and four l's have been received. To decode the four supervisory characters it is only necessary to find the position of the other three 1's. NAND gates A2A9U1B, U1A, U2A, U2B (Figure A -6) are connected to the constant ratio parallel lines to test for the four supervisory con, binations; when true, they generate a LOW signal at last bit time. The supervisory characters SYNC A and SYNC B are always transmitted together and form a sequence of eight l's followed by four or seven 0's; this combination is found only in the resynchronization sequence. The receiver must be able to detect this unique sequence at any bit time in order to generate a resynchronization sequence is described in paragraph 4-11. NAND gate A2A9U8A (Figure A -6) tests the first four constant ratio signal lines; if four sequential l's are detected its output goes LOW generating the signal SYNC A RCVD, which starts counter AZA11U8 (Figure A-18) in the Sync Pattern Detector (RCVR 21) logic. This counter counts 8 bit times for 8-bit constant ratio codes and 11-bit times for 11-bit constant ratio codes. The position of the four l's for the SYNC B supervisory character depends upon the length of the constant ratio code in use; the gates A2A9U19A (Figure A-4) U8B (Figure A-6), U20C, U20D, (Figure A -2) with the control signal CODE 8 BIT, select the correct constant ratio lines. If four consecutive l's are detected, the output (Pin 11) of NAND gate A2A9U20D goes LOW generating the signal SYNC B RCVD. This is tested by the Sync Pattern Detector (RCVR 21) during the last count of counter A2A11U8 (Figure A-18). If the signal SYNC B RCVD is true (LOW) during the last count, eight consecutive l's followed by one 0 have been received. To more fully decode the supervisory character SYNC B NAND gate U19B (Figure A-4) test three more of the O's that should follow the eight consecutive l's and, if true, the receiver forces a new last bit time and starts a resynchronization sequence.

o. Constant Ratio Code Decoding. - The constant ratio codes are decoded by-the Constant Ratio Decoder (RCVR 17), which consists of two 256 x 4-bit Read Only Memories (ROM's). These decode 256 different 11-bit constant ratio codes into the 256 8-bit terminal codes received by the distant transmitter. The conversion is stored with the constant ratio code forming the

address to the two ROM's and the 8-bit terminal code king the contents of each ROM at the selected address.

p. Serial Data Transmission. - The output of the decoder is loaded into the the Parallel-To-Serial Converter (RCVR 18) during last bit time by the timing signal R N2 CLK, which occurs 6 microseconds after the signal R N1 CLK. The output terminal code is shifted out bit by bit as a new constant ratio code is being shifted in. As the terminal code is being shifted out of the parallel-to-serial converter l's are shifted into the serial inputs (Pins 2 and 3) of A2A9U3 (Figure A-20) to form the stop bits (always HIGH). The different length terminal codes are selected by NAND gates A2A9U6A, U6B, U6C, U6D (Figure A-2), and by control signals 8 BIT S-S, 7 BIT S-S, 6 BIT S-S, and CODE 8 BIT. In 8-bit start-stop an extra flip-flop A2A9U4B (Figure A-14) is used to generate the start bit (always LOW); in all other start-stop modes the start bit is included in the decoded constant ratio terminal code. Each character transmitted with an 11-bit constant ratio code requires 11 bit times, and extra stop bits are added to make up the required time. Likewise, with an 8-bit constant ratio code all characters require 8 bit times.

q. Data Flow lnhibit. - The output signal from the parallel-to-serial converter can be inhibited by the Data Inhibit (RCVR 19) logic if the control signal R OUT EN is false (LOW) or R IDL DA INH is true (LOW) forcing the output to be constantly HIGH, which halts the data sink. To assist with the data sink timing--particularly in the bit stream mode--the receiver also generates step clock. In start-stop modes this consists of a single pulse once per character during the last bit time. In bit stream mode however the receiver step clock is six cycles of the receiver clock and the center of each data bit occurs at the fall of the step clock.

r. Data Timing. - The output data signal R O DA A is retimed to the receiver clock R CLK by the Output Data Retimer (RCVR 11) logic and then converted to bipolar LOW level dc interface signal R O DA L by the Line Driver (RCVR 31). The receiver step clock signal is also converted into a bipolar LOW level dc interface signal R CLK ST L by the Line Driver (RCVR 29).

s. Receiver Indicator. - The receiver also generates an indicator signal to the data sink when a mutilated character has been received. This signal is also transmitted by a LOW level dc interface using the Line Driver (RCVR 30) and the signal MC IND L.

4-10. ARQ CYCLE. - The ARQ cycIe is an automatic retransmission of a sequence of data that occurs when the receiver detects an error in transmission. The actual number of characters that are retransmitted in both directions depends upon the memory length selected, which is determined from the propagation delay between the transmitter and receiver.

a. ARQ Initiation. - The ARQ cycle is initiated by the receiver when it detects an error in transmission or when commanded by an ARQ supervisory control character. Consider first the mutilated character logic in the receiver. A character is deemed mutilated if it is not a constant ratio code (does not have four l's) or if it is an unused constant ratio code combination. Both result from errors in transmission, The receiver generates two control signals NCR RCVD and UNUSED RCVD, which are logically OR'ed in the mutilated character indicator (RCVR 20) by the NOR gate A2A11U14A, and tested at the receiver last bit time by NAND gate A2A11U14B. If a mutilated character is received, the output (Pin 6) of U14B goes LOW. This sets the J input (Pin 14) of flip-flop A2A11U20A HIGH via inverter A2A11U16C and at the fall of the receiver clock signal R CLK the mutilated character indicator is illuminated. The indicator signal also resets the Two ARQ's Detector (RCVR 22) latch A2A11U24B making the signal TWO ARQ'S RCVD false (LOW). The two control signals NCR RCVD and UNUSED RCVD are also logically OR'ed in the ARQ flag logic (RCVR 26) together with the control signals ARQ RCVD and TWO ARQ'S RCVD by the NOR gate A2A11U22B, then logically AND'ed with the receiver last bit time and the control signal ARQ CYCLE (which indicates that the receiver is not processing an ARQ cycle) by the NAND gate A2A11 U15B. Thus, if a mutilated character is received, or if the ARQ supervisory control character is received during the receiver last bit time when the receiver is not already processing an ARQ cycle, the output of NAND gate A2A11U15B (Pin 6) goes LOW. To hold the system in ARQ during a resynchronization sequence this signal is logically OR'ed with control signals X SYNCING and R SYNCING by the NOR gate A2A11U22A setting the J input (Pin 7) of flip-flop A2A11U22B HIGH. This signal is inverted by A2A11U10C, then logically OR'ed with the control signal ARQ CYCLE {which is true (LOW) when the receiver is processing an ARQ cycle) by NOR gate A2A11U9C to generate the control signal R IN ARQ. This enables NAND gate A2A11U11A and disables the receiver Inhibit ACTIVATE flag (RCVR 27). The signal R IN ARQ is inverted by inverter A2A11U19F to generate the ARQ cycle counter (RCVR 24) output signal R IN ARQ, which inhibits the output data to the data sink.

b. Setting the ARQ Flag. - The next timing signal R L N1 CLK, which occurs at the end of the receiver last bit time, presets the ARQ flag flip-flop A2A11U20B and loads the ARQ character counter A2A11U3 (with a number dependent upon the memory length selected) via NAND gate U11A. This sets the control signal ARQ CYCLE true (LOW) and enables the ARQ counter to count. The timing signal R L N2 CLK, which occurs at the beginning of the receiver last bit time resets flip-flop A2A11U18A. This disables NAND gate A2A11U11A (preventing the counter being reloaded or the ARQ flag flip-flop being reclocked) and increments the ARQ counter via gates A2A11U9B and A2A11U10E. The ARQ counter continues to count characters (all disabled from the data sink in response to control signal R IN ARQ until maximum count is reached. (The number of characters required is the same as the

transmitter memory length.) The control signal ARQ CYCLE is false (HIGH) at maximum count of the ARQ counter and NAND gate A2A11U15B is enabled to test if the incoming character is mutilated. If not, and two ARQ supervisory characters have been received during the ARQ sequence, the receiver leaves the ARQ cycle and resumes normal data flow, allowing the tested character to go to the data sink.

c. Transmitter Response to the ARQ Flag. - The transmitter detects the receiver ARQ flag with the timing signal X NL CLK, which occurs at the center of the transmitter last bit time. If the receiver flag signal R ARQ FLG is set, it presets flip-flop A2A4U10B, and its Q output (Pin 5) goes HIGH. This is applied to the D input of flip-flop A2A4U5A. It also enables the Sync Initiate block (XMTR 26) with the signal ARQ SYNC EN. The Q output (Pin 6) of A2A4U10B goes LOW generating the control signal X ARQ INH, which holds the transmitter step clock and disables the Inhibit Request block (XMTR 23). This signal also generates the memory ARQ marker bit MEM IN 9 via the enabled NAND gate A2A4U6B and sets the D input (Pin 12) of flip-flop A2A4 U11B to be LOW. At this tine memory write signals MEM WRITE A and MEM WRITE B write the last data character and the ARQ marker bit MEM IN 9 into the memory, which responds with the signal MEM OUT 9 true (LOW). This signal, via NOR gate A2A4U12C, makes the D input (Pin 12) of flip--flop A2A4U11A HIGH. It also enables NAND gate A2A4U6B via NOR gate A2A4U6A and inhibits the generation of a Sync Cycle from the front panel SYNC initiate switch. The timing signal X PL CLK then resets flip-flop A2A4U11B; output Q (Pin 9) goes LOW producing the ARQ supervisory inhibit signal ARQ SUP INH. Flip-flops A2A4U18A and A2A4U11A are preset by X PL CLK. Output Q (Pin 5) of U11A goes HIGH generating the supervisory control signal ARQ GEN via inverter A2A4U17A. Output Q (Pin 6) goes LOW disabling NAND gate A2A4U1D and generating the ARQ flag clear signal X CL ARQ FLG, which clears the receiver ARQ flag. The Q output (Pin 6) of flip-flop U18A goes LOW holding the D input (Pin 2) on U11A HIGH via NOR gate A2A4U12.

d. Transmitter Character Counter. - The transmitter timing signal X PL CLK also increments the memory address counter, which removes the ARQ marker bit, and the signal MEM OUT 9 becomes false (HIGH). This makes the D input (Pin 2) of A2A4U18A LOW and removes the second enable on NAND gate A2A4U6B via NOR gate A2A4U6A. It also enables the front panel SYNC initiate switch as FP SYNC INH becomes false (LOW). At the end of the next character the transmitter timing signal X NL CLK presets flip -flop A2A4U5A. Its Q output (Pin 5) goes HIGH, sets the D input (Pin 12) of A2A4U5B HlGH, and enables NAND gate A2A4U1D (second input to U1D is disabled by A2A4U11A). Its Q output (Pin 6) disables NAND gate A2A4U6B (via U6A). Pin 4 goes LOW, removing ARQ marker bit signal MEM lN 9. The J-K flip-flop A2A4U10B has both J and K inputs LOW because the ARQ flag signal has been reset (LOW) and the memory out signal MEM OUT 9 is false (HIGH). Therefore its output does not change when clocked. At this

time memory write pulse MEM WRITE B writes the generated ARQ supervisory character into memory; this is followed by the next rise of transmitter clock X CLK-1, which presets flip-flop A2A4U5B. Its Q output (Pin 9) goes HIGH, and lights the front panel indicator lamp ARQ CYCLE via the driver inverter A2A4U3D and resistor R5. The output of inverter A2A4U3D also generates the remote signal ARQ IND. The next transmitter timing signal X PL CLK resets flip-flop A2A4U18A causing the D input (Pin 2) of flip-flop A2A4U11A to be set LOW. The memory address counter is also incremented at this time by the X PL CLK signal. At the end of the next character the timing signal X NL CLK has no effect and the next memory write signal MEM WRITE B writes a second ARQ supervisory character into the memory. The X PL CLK signal then resets A2A4U11A, which disables the supervisory generator signal ARQ GEN and removes the clear signal X CL ARQ FLG from the receiver ARQ flag. At the same time it enables NAND gate U1D to generate the inhibit signal MEM ARQ INH. This disables the memory write signal MEM WRITE B, and the memory parity checker.

e. Retransmission From Memory. - With the memory write signal disabled, the transmitter continues to transmit data characters that were previously stored in the memory. No new data is accepted from the data source, or supervisory characters generated. The memory address counter is incremented after each character has been transmitted; after one complete memory cycle, the ARQ marker bit MEM OUT 9 again becomes true (LOW). The character accepted at the time of the ARQ flag is now on the memory output lines and the receiver may have repeated the ARQ flag. If so, the transmitter repeats the ARQ sequence. The effect of the marker bit MEM OUT 9 on flip-flop A2A4U10B nullified by the raised receiver flag signal R ARQ FLG. and it remains preset. The memory signal MEM OUT 9 is inverted by U17C and enables NAND gate A2A4U6B via NOR gate A2A4U6A to generate the ARQ marker bit MEM IN 9, which is written into the same memory address by the signal MEM WRITE A. The transmitter repeats the ARQ sequence, generating two ARQ supervisory characters, clearing the receiver ARQ flag, and repeating the contents of its memory.

f. Return To Normal Data Flow. - If the receiver has not raised the ARQ flag at the end of the last memory character, the timing signal X NL CLK resets flip-flops A2A4U10B, which removes the inhibit from the transmitter step clock by making the signal X ARQ INH false (HIGH), and setting the D input (Pin 12) of flip-flop A2A4U11B HIGH. At this time X PL CLK sets A2A4U11B; its Q output (Pin 9) goes HIGH disabling the signal ARQ SUP INH. The D input (Pin 2) of flip-flop A2A4U5A is set LOW by the Q output of A2A4 U10B. At memory write time, MEM WRITE B is still disabled and the last character is transmitted from the memory. Also the ARQ marker bit MEM OUT 9 is erased because MEM WRITE A is never disabled and MEM IN 9 is set LOW because NAND gate A2A4U6B is disabled and X ARQ INH is false (HIGH). The transmitter now requests a new data character from the data

source with a step clock signal X ST CLK and converts it into a parallel combination. The next X NL CLK clock signal resets flip-flop U5A, disabling NAND gate U1D, and removes the memory write inhibit signal MEM ARQ INH The D input (Pin 12) of flip-flop A2A4U5B is also set LOW at this time. The memory write signal MEM WRITE B writes the new character into the memory and the transmitter transmits it. The next rise of the transmitter clock X CLK 1 resets flip-flop A2A4U5B, which extinguishes the front panel ARQ INDICATOR light and makes the remote signal ARQ IND false (HIGH). The transmitter ARQ sequence has now returned to Normal Data Flow.

4-11. SYNCHRONIZATION CYCLE. - If the AN/FYC-12 communication system is locked up in a repeating ARQ cycle, the synchronization between transmitter and receiver in both directions is automatically corrected when the operator at either end of the system initiates a resynchronization sequence. This is called a sync cycle and can be initiated only when the system is in a repeating ARQ cycle.

a. Initiation by Operator. - The operator operates the SYNC initiate switch generating the signals FP SYNC INT and FP SYNC INT, which are de-glitched by the R -S flip-flop consisting of A2A4U1A and A2A4U7A, then logically OR'ed to the remote sync initiate signal SYNC INT by the negative logic NOR gate A2A4U1B. The output (Pin 6) goes HIGH to initiate a sync cycle. This signal is applied to the J input (Pin 1) of flip-flop A2A4U8A, and its complement--generated by inverter A2A4U16F--is applied to the K input (Pin 4). A2A4U8A and A2A4U8B are normally reset (both Q outputs LOW), thus disabling NAND gate A2A4U7C. When a sync cycle is initiated, the J input (Pin 1) of A2A4U8A is HIGH. At the end of the active character, timing signal X NL CLK presets A2A4U8A; its Q output (Pin 3) goes HIGH, which--if the system is in an ARQ cycle--enables NAND gate A2A4U7C to generate the sync cycle start signal ST SYNC CYCLE at its output (Pin 8). This signal is inverted by A2A4U2A and becomes the J input (Pin 8) of flip-flop A2A4U8B, which is preset at the end of the next character by the timing signal X NL CLK and removes ST SYNC CYCLE.

b. Initiation By Receiver Flag. - The signal ST SYNC CYCLE is logically OR'ed with the receiver flag signal R SYNC FLG 1 (which is active if the receiver has received a resynchronization sequence from the distant transmitter) by the negative logic NOR gate A2A4U3B and its output (Pin 6) becomes the J input (Pin 1) of the flip-flop A2A4U10A. This is clocked at the end of the active character by the timing signal X NL CLK; its Q output (Pin 2) goes LOW generating control signal X SYNCING, which enables NAND gate A2A4U9B to generate sync cycle memory marker bit MEM IN 10. The same signal disables NAND gate A2A4U1C and sets LOW the D input (Pin 2) of flip-flop A2A4C14A. The Q output of A2A4U10A goes HIGH and is directly con - nected to the D input (Pin 12) of A2A4U4B. At this time memory write signal MEM WRITE A writes the sync cycle marker bit MEM IN 10 into the memory,

which generates the signal MEM OUT 10. This adds a second enable to NAND gate A2A4U9B via inverter A2A4U17D and NOR gate A2A4U6C. Three microseconds later X L PS CLK presets flip-flop A2A4U4B. Its Q output (Pin 9) generates the start sync sequence signal ST SYNC SEQ and enables input (Pin 9) of NAND gate A2A4U1C; but input (Pin 10) is disabled by the signal X SYNCING, which prevents the receiver flags being cleared at this time. its Q output removes the first enable from A2A4U9B via NOR gate A2A4U6C. The rise of the transmitter clock signal X CLK 1 resets A2A4U4A; it Q output goes LOW, and through NOR gate A2A4U2C and driver inverter A2A4U3F lights the front panel indicator SYNC and generates the remote signal SYNC IND.

C. Character Count By Incrementing Memory. - The next timing signal X PL CLK increments the memory address counter, removing the sync cycle marker bit MEM OUT 10. It also clocks flip-flop A2A5U7B, which disables the memory output data via transmitter block (XMTR 29), and enables flip-flop A2A4U14A (XMTR 28) to generate the sync supervisor character SYNC A. This is transmitted as the next character but not memorized. During the last bit time the timing signal X PL CLK again increments the memory, presets flip-flop A2A4U14B, and resets flip-flop A2A4U14A, which generates the sync supervisory character SYNC B. This is also transmitted to complete the special synchronization sequence of eight l's followed by four or seven 0's. The memory is again incremented by X PL CLK and flip-flop A2A4U14A is preset to generate the sync supervisory character Inhibit ACTIVATE or Inhibit DEACTIVATE (depending upon the position of the INHIBIT switch or remote line). The transmitter continues to transmit the inhibit supervisory characters until the sync cycle memory marker bit is detected after one complete memory length. At this time the transmitter tests the receiver sync flags to check that it has received the resynchronization pattern and has resynchronized (R SYNC FLG 1 true (LOW)) and that it has afterwards correctly received the Inhibit ACTIVATE or Inhibit DEACTIVATE supervisory characters (R SYNC FLG 2 true (LOW)). If both flags are true (LOW), the next X NL CLK resets (toggles) flip-flop A2A4U10A, which removes the signal X SYNCING and resets both the receiver sync flags via NAND gate A2A4 U1C. The D input (Pin 2) of flip-flop A2A4U4A is also set HIGH and the sync cycle marker bit MEM IN 10 is set LOW via the NAND gate A2A4U9B at this time. The last inhibit supervisory character is now transmitted and the sync cycle marker bit MEM IN 10 is erased from memory A. Flip-flop A2A4U4B is reset by the timing signal X L PS CLK, which removes the control signal ST SYNC SEQ. The next timing signal X PL, CLK Increments the memory address counter and removes the inhibit from the memory output lines by clocking flip-flop A2A5U7B Flip-flops A2A4U14A and A2A4U14B are both reset at this time and the transmitter resumes the ARQ cycle, transmitting characters from memory. The rise of tie transmitter clock signal X CLK 1 presets flip-flop A2A4U4A, which removes the transmitter hold on the sync cycle indicator signals. If the two receiver sync flags R SYNC FLG 1 and

R SYNC FLG 2 are not true (LOW) when the sync cycle marker bit MEM OUT 10 becomes LOW, the transmitter repeats the resynchronization sequence.

d. Receiver Synchronization. - The receiver is always searching for the resynchronization pattern of eight consecutive 1's followed by four or seven 0's. NAND gate A2A9U8A tests the incoming data for four consecutive 1's, which might be the supervisory character SYNC A, and generates the control signal SYNC A RCVD; this starts a counter A2A11U18, which counts one constant ratio character - -either 8 or 11 bit times depending upon format selected. If the four sequential bits detected by NAND gate A2A9U8A are part of the supervisory character SYNC A, then--after counting one complete con - stant ratio character (8 or 11 bits)--the supervisory character SYNC B appears on the data lines. The gates A2A9U8B, A2A9U19A, A2A9U20C, and A2A9U20D detect the four 1's in the two different length formats and generate the signal SYNC B RCVD. Gates A2A9U15A, A2A9U15E, A2A9U15F, and A2A9U19B detect three of the following 0's and generate the signal SYNC 0 RCVD. If both are true (LOW) when counter A2A11U8 has counted one complete constant ratio character after detecting the signal SYNC A, the receiver assumes that it has received the resynchronization pattern and forces the present bit time to be last bit time with the signal R RESYNC. This signal also sets the receiver sync flag R SYNC FLG 1, which requests the transmitter to transmit a sync sequence to the distant receiver, if it is not already so engaged. R SYNC FLG 1 starts the sync counter A2A11U1 and A2A11U2 which holds the complete system in ARQ for at least two memory cycles by generating the control signal R SYNCING.

e. Return to ARQ Cycle. - After resynchronization the receiver tests the characters that follow. If the Inhibit ACTIVATE or the Inhibit DEACTIVATE supervisory characters are detected, it sets the second receiver sync flag R SYNC FLG 2 LOW to indicate that it has successfully resynchronized. The transmitter requires that both flags be LOW before it can leave the resynchronization sequence.

4-12. INHIBIT OPERATION. - The operator at the receiving end of the system can control the distant transmitter with the inhibit supervisory characters, The Inhibit ACTIVATE supervisory character lights the INHIBIT RCVD indicator at the distant end and, if Option A is selected, close down the distant data source by inhibiting the transmitter step clock. The Inhibit DEACTlVATE supervisory character extinguishes the INHIBIT RCVD indicator and enables the distant data source.

a. Generation of Inhibit Supervisory Characters. - The inhibit supervisory characters are generated with the INHIBIT ACTIVATE/DEACTIVATE switch on the front panel, or with the remote LOW level dc interface line LOCAL END INH L signal, which--when HIGH--generates the Inhibit ACTIVATE, and

when LOW generates the Inhibit DEACTIVATE. The generation of either inhibit supervisory character is disabled if the system is performing an ARQ or SYNC sequence. Inhibiting is accomplished by the signals X ARQ INH and X SYNCING using negative logic NOR gate A2A3U16D and NAND gates A2A3 U17A and A2A3U17B. The signals from the INHIBIT ACTIVATE/DEACTIVATE switch are de-glitched by an R-S flip-flop consisting of A2A3U9B and A2A3U9C and logically OR'ed with the remote signal LOCAL INH in A2A3 U16A. Two flip-flops, A2A3U18A and A2A3U18B, form a transient detector that tests for a change in the position of the switch or in the state of the remote line LOCAL INH at the transmitter last bit time. (Timing signal X L PS CLK occurs 3 microseconds after a memory write pulse.) If a change has occurred, the transmitter step clock is halted for one character time by the signal INH SUP INH, and the signals INH ACT GEN or INH DEACT GEN generated depending upon the new position of the switch or state of the remote line, thus generating the required supervisory character. In addition, flip-flop A2A3U3 is preset by the transmitter clock X CLK when the Inhibit ACTIVATE is transmitted, and lights the front panel indicator INHIBIT REQ. The flip-flop is reset when the Inhibit DEACTIVATE is transmitted, which extinguishes the indicator INHIBIT REQ. The signal SWITCH INH A/D which is LOW when an Inhibit DEACTIVATE is requested and HIGH for an Inhibit ACTIVATE, is generated by flip-flop A2A3U18A; it determines which of the inhibit supervisory characters is transmitted when the data source is closed down because the local receiver has received the Inhibit ACTIVATE supervisory character with the strap option in position A.

b. Reception of Inhibit Supervisory Characters. - If the system is not in an ARQ or SYNC cycle, the receiver sets the inhibit flag INH ACT FLG (HIGH) when it receives the Inhibit ACTIVATE supervisory character and (LOW) when it receives inhibit ACTIVATE flag. The flag consists of flip-flop A2A11U13A and is clocked by the timing signal R L N2 CLK via NAND gate A2A11U5D and inverter A2A11U5C.

c. Transmitter Response to Receiver Flag, - The transmitter tests the receiver inhibit flag signal R lNH ACT FLG at the end of every character using the flip-flop A2A3U8A and timing signal X NL CLK. If the flag is set (HIGH), flip-flop A2A3U8A is preset, its Q output (Pin 5) is HIGH making the D input of flip-flop A2A3U8B also HIGH. If the strap option plug is set for Option A, NAND gate A2A3U9D is enabled and control signal X DA INH RCVD becomes true (LOW), which disables the transmitter step clock. Flip-flop A2A3U8B is preset by the transmitter clock signal X CLK, lighting the front panel indicator R DIST INH and generating the remote signal R DIST INH IND. Timing signal X PL CLK resets the flip-flop A2A3U1A, which generates the signal INH GEN enabling the memorized supervisory generator to generate either the ACTIVATE or DEACTIVATE supervisory character, depending upon the state of control signal SWITCH INH A/D. If strap option B is selected

NAND gate A2A3U9D is disabled and only the indicator light is enabled; the data source continues to transmit, and must be manually halted.

d. Return to Normal Data Flow. - The transmitter continues to test the receiver inhibit flag at the end of every character; when reset (LOW), flip-flop A2A3U8A is reset; it's Q output (Pin 5) goes LOW setting the D input (Pin 12) of A2A3U8B also LOW, disabling NAND gate A2A3U9D. The next transmitter clock X CLK extinguishes the front panel indicator and resets remote line signal R DIST INH IND. If option A is selected, timing signal X PL CLK presets flip-flop A2A3U1A removing the inhibit generate signal INH GEN.

4-13. POWER DISTRIBUTION. - The low voltage power for the transmitter and receiver logic is supplied by the dc-dc converter (assembly A2A17). This plug-in assembly converts the ±6-volt (or 12-volt) supply potentials into the regulated voltages required. It is protected from overload by a 6-amp circuit breaker (power switch CB1) and from reverse polarity by an internal diode that trips the circuit breaker if the supply is incorrectly connected.

a, Voltages. - The output voltages are 5 volts ±5% and ±12 volts ±15%. All the outputs are protected against short circuit and overvoltage, and re-cover automatically when the short circuit or overvoltage is removed. The S-volt output can be adjusted over a ±5% tolerance but the ±12-volt output is preset at the factory.

b. Distribution. - The 5-volt output is used to power all the TTL logic modules and light the indicators. The ±12-volt output is used to power the line drivers that convert the TTL signals into ±6-volt bipolar LOW level dc interface signals. The -12-volt and +5-volt outputs power the line receivers that convert the bipolar input signals into TTL compatible signals.

c. Grounding. - To minimize ground loops the only ground connection to the chassis (main frame) is made within the &-dc converter assembly. The common for the ±12-volt output used by the external LOW level dc interface is isolated from the TTL common and connected to ground within the dc -dc converter assembly.

IV - CIRCUIT DESCRIPTION

4-14. TRANSMITTER. - This section describes the overall functions of the transmitter; the logic functions of each block are described in detail to enable a proper understanding of the transmitter operation. Reference is made throughout the following discussion to the appropriate top level and subsystem block diagrams, and the transmitter timing diagrams. The AN/FYC-12 transmitter receives data characters from the data source via low level (MIL STD 188C) circuit, enters them into memory, encodes them into constant ratio codes, and adds supervisory characters. These may cause the distant receiver to request a retransmission (ARQ), to halt transmission (Inhibit Activate), or to resynchronize (Sync A and Sync B) before transmitting the encoded data again via a low level transmission circuit. The logic components for the AN/FYC-12 transmitter are contained on eight circuit boards:

1. A2A1 Data Sample Generator
2. A2A2 Fast Clock Step Generator
3. A2A3 Inhibit Control XMTR Clock Generator
4. A2A4 XMTR ARQ and SYNC Control
5. A2A5 Constant Ratio Code Generator
6. A2A6 Data Input Code and Memory Counter
7. A2A7 Recirculating Memory
8. A2A8 Level Converter

To help understand the complex logic, the functions of each circuit card are reduced to logical blocks, which are described in detail. The logical blocks for the transmitter circuit boards are:

1. A2A8 Level Converter (Figure A-36)
   a. XMTR 1 Incoming Data Line Receiver
   b. XMTR 2 Station Clock Line Receiver
   c. XMTR 3 Sync Initiate Line Receiver
   d. XMTR 4 Local Inhibit Line Receiver
   e. XMTR 44 Outgoing Data Line Driver
   f. XMTR 45 Sync Cycle Indicator Line Driver
   g. XMTR 46 Transmitter Step Clock Line Driver
   h. XMTR 47 ARQ Cycle Indicator Line Driver
   i. XMTR 48 Distant Inhibit Request Line Driver

2. A2A1 Data Sample Generator (Figure A -40)
    a. XMTR 5 Start Pulse Detector
    b. XMTR 6 Serial-To-Parallel Clock Generator
    c. XMTR 7 Sample Time Counter
    d. XMTR 8 Sample Comparator
    e. XMTR 9 Reference Time Counter
    f. XMTR 10 Sample Enable
    g. XMTR 11 Clock Step Inhibit

3. A2A2 Fast Clock Step Generator (Figure A-41)
    a. XMTR 12 Fast Clock Generator
    b. XMTR 13 Initialize Logic
    c. XMTR 14 Data Window Logic
    d. XMTR 15 XMTR Bit Counter
    e. XMTR 16 XMTR Last Bit Counter
    f. XMTR 17 Bit 6A Generator

4. A2A3 Inhibit Control XMTR Clock Generator (Figure A-42)
    a. XMTR 18 XMTR Clock Generator
    b. XMTR 19 XMTR Last Clock Generator
    c. XMTR 20 Clock Step Generator
    d. XMTR 21 Parallel-To-Serial Clock Generator
    e. XMTR 22 Inhibit Received Control
    f. XMTR 23 Inhibit Request Control
    g. XMTR 24 Memory Write Control

5. A2A4 XMTR ARQ and SYNC ControI (Figure A-43)
    a. XMTR 25 XMTR ARQ Cycle Control
    b. XMTR 26 SYNC Initiate
    c. XMTR 27 XMTR SYNC CycIe Control
    d. XMTR 28 Sync Cycle Supervisor Control

6. A2A5 Constant Ratio Code Generator (Figure A-44)

a. XMTR 29 Sync Cycle Data Inhibit

b. XMTR 30 Sync Cycle Activate or Deactivate Generator

c. XMTR 31 Constant Ratio Code Encoder

d. XMTR 32 Sync Cycle SYNC A and SYNC B Generator

e. XMTR 33 Parallel-To-Serial Converter

f. XMTR 34 Format Switch Decoder

7. A2A6 Data Input Code and Memory Counter (Figure A-45)

a. XMTR 35 Serial-To-Parallel Converter

b. XMTR 36 Memorized Supervisor Data Inhibit

c. XMTR 37 Memorized Supervisor Generator

d. XMTR 38 Memorized Supervisor Control

e. XMTR 39 Memory Address Counter

8. A2A7 Recirculating Memory (Figure A-46)

a. XMTR 40 Memory "A"

b. XMTR 41 Memory "B"

c. XMTR 42 Parity Generator

d. XMTR 43 Parity Checker

The following is a description of each logic block, starting with the first block on Level Converter A2A8. The function of the logic is detailed; then a signal-by-signal description is given. It will be helpful to refer to the Transmitter Signal Name Glossary (Table 6-2) and the applicable circuit board logic diagrams.

a. A2A8 Level Converter (Logic Diagram Figure A-47 Block Diagram Figure A-36, Wiring Diagram Figure A-74).

(1) XMTR 1 Incoming Data Line Receiver. - This block converts the incoming bipolar (MIL STD 188C) low level interface signal into a TTL compatible signal. The conversion is accomplished by an integrated circuit, Dual Interface Receiver U1A, which is described in Figure A-13. The incoming data signal X IN DA L line and its return X IN DAL R is converted into the TTL signal $\overline{\text{X IN DA}}$ and then inverted by U4A to generate the output signal X IN DA at Pin 12 of U4A (Figure A-1).

(2) XMTR 2 Station Clock Line Receiver. - This block converts the incoming Station clock, which will be called the Transmitter Clock, from bipolar to TTL, compatible signal. Referring to Figure A-47, the same integrated circuit U1B (Figure A-13) as used for the incoming data is also used for the incoming clock (the clock is at twice the data rate). The incoming station clock signal X CLK L and its return X CLK L R are converted into the TTL signal X CLK by U1B. Output is monitored at TP1.

(3) XMTR 3 Sync Initiate Line Receiver. - This block converts the remote Sync initiate control signal from bipolar to TTL compatible form. The control signal SYNC INL L and its return SYNC INT L R are converted to the TTL signal SYNC INT by U2A (Figure A-13).

(4) XMTR 4 Local Inhibit Line Receiver. - This block converts the remote local inhibit activate control signal from bipolar to TTL compatible form. The control signal LOCAL END INH L and its return LOCAL END INH L R are converted into the TTL signal LOCAL INH by U2B (Figure A-13).

(5) XMTR 44 Outgoing Data Line Driver. - This block converts the TTL outgoing data signal into a bipolar (MIL STD 188C low level interface) signal. The conversion (including voltage and current limiting) is accomplished by an integrated circuit, Dual interface transmitter U6B, which is described in Figure A -12. The waveshape of the output signal is controlled by the discrete capacitor C12, the capacitance of which depends upon the baud rate in use. The factory installed value of C12 is 0.0056 µF; this is the value for the highest baud rate of 9600 baud. The TTL data signal SND LIN is converted to the bipolar signal SND LIN L with a common return line OUT SIG RTN. As shown in the logic diagram the dual interface transmitter integrated circuit inverts the data. The output of this block--bipolar signal SND LIN L--can be monitored at TP6.

(6) XMTR 45 Sync Cycle Indicator Line Driver. - This block converts the TTL Sync cycle indicator signal into a bipolar low level interface signal suitable for transmission to the data control room. The TTL signal SYNC IND is converted into the bipolar signal SYNC IND L with common return line OUT SIG RTN by integrated circuit U7A (Figure A-12). The waveshape is controlled by C13.

(7) XMTR 46 Transmitter Step Clock Line Driver. - This block converts the TTL step clock signal into a bipolar low level interface signal. The TTL signal X CLK ST is applied to the input of U8B (Figure A-12), which generates the bipolar signal X CLK ST L, with common return line OUT SIG RTN. The wave shape of this signal is controlled by C 16, and it can be monitored at test point TP7.

(8) XMTR 47 ARQ Cycle Indicator Line Driver. - This block converts the TTL ARQ cycle indicator signal into a bipolar low level interface signal suitable for transmission to the data control room. The TTL signal ARQ IND is converted to the bipolar signal ARQ IND L (with common return OUT SIG RTN) by U7B (Figure A-12); C14 is used to control the wave shape.

(9) XMTR 48 Distant Inhibit Request Line Driver. - This block converts the TTL received distant inhibit activate indicator signal into a bipolar low level interface signal suitable for transmission to the data control room. The TTL signal R DIST INH IND is converted to the bipolar signal R DIST INH L with common return OUT SIG RTN by U8A (Figure A-12); C15 is used to control the wave shape.

b. A2A1 Data Sample Generator (Logic Diagram Figure A -40, Block Diagram Figure A29, Wiring Diagram Figure A-67, Timing Diagrams Figures A -59 and A -64).

(1) XMTR 5 Start Pulse Detector. - The purpose of this block is to detect and time the start bit (first bit of each character--always LOW in all start-stop modes) and to generate the signal X ST BIT DET. This block is used only in start-stop modes of operation; in bit stream no start bit is transmitted. The block consists of three flip-flops, U7B (Figure A-16), U8A, and U8B (Figure A-14); three NAND gates U9A (Figure A-2), U16D (Figure A-2) U15B (Figure A-6); one inverter U9B (Figure A-2); and one NOR gate U16A (Figure A-2). The three flip-flops form a 3-bit shift register--clocked by the fast clock signal FAST CLK. The incoming data signal X IN DA is applied to the signal input (Pin 12) of U7B and shifted into U8B and U8A by successive fast clock pulses. The logic diagram shows that the delayed data signal X IN DA DL is taken from Q (Pin 8) of U8B; it is delayed two fast clock periods (12 micro-seconds approximately).

(a) Consider the system working in any start-stop mode: the control signal BIT STREAM is false (HIGH); during the stop bit--when the incoming data signal X IN DA is HIGH--flip-flop U7B is set (Q = HIGH). U8A and U8B are both reset (Q = LOW). The timing signal SMPL WDO is true (HIGH) during the first two bit times of the transmitter timing sequence; this enables NAND gate U15B to detect a start bit only during this time. The output signals $\overline{Q}$ (U7B) and $\overline{Q}$ (U8A) are also connected to NAND gate U15B, together with the control signal BIT STREAM. After the stop pulse has been detected, the output of U7B $\overline{Q}$ (Pin 8) is LOW: but the output of U8A $\overline{Q}$ (Pin 6) is HIGH, hence, during the first two transmitter bit times--when SMPL WDO is true (HIGH)--NAND gate U15B is disabled only by the output of U7B $\overline{Q}$ (Pin 8). When the incoming data signal X IN DA goes LOW for the start bit of the next character, flip-flop U7B is reset on the next fast clock; $\overline{Q}$ (Pin 8) goes HIGH and enables NAND gate U15B. Its output (Pin 8) goes LOW, generating the output signal

X ST BIT DET. After two more periods of the fast clock (12 microseconds) flip-flop U8A is set forcing output Q (Pin 6) LOW, disabling NAND gate U15B, and removing the signal X ST BIT DET. Thus, when a start bit is detected, the signal X ST BIT DET goes true (LOW) for two fast clock periods (12 microseconds) at the beginning of the bit time.

(b) In bit stream mode NAND gate 15B is permanently disabled by control signal BIT STREAM on Pin 9, which prevents the generation of X ST BIT DET.

(c) The start pulse detector also generates the control signal X ST SMPL EN, which starts the sample enable sequence. In start-stop modes this signal is the same as X ST BIT DET, but inverted by the negative logic NOR gate U16A. In bit stream mode it is the one-bit-wide sample window signal--SMPL WDO--enabled by NAND gate U16D and logically OR'ed to the start-stop mode signal by negative logic NOR gate U16A. The NAND gate U9A and control signal INHIBIT GEN prevents the enabling of an extra character during the initialization sequence, which would cause an ARQ lock-up condition.

(d) The incoming data signal X IN DA and the output signal X ST BIT DET can be monitored at test points TP4 and TP8 respectively.

(2) XMTR 6 Serial-To-Parallel Clock Generator. - The purpose of this block is to generate the two timing signals X SP CLK and X SMPL CTR CLK; both occur at the center of the incoming data bits and have a duration of one half a fast clock period (3 microseconds). The block consists of two NAND gates U9C and U9D (Figure A -2) and an inverter U2B (Figure A-1). The timing signal X SP CLK TM is always at the center of the incoming data bits; it has a duration of one fast clock period (6 microseconds), and it occurs once per transmitter bit time (8 or 11 bits per character). This timing signal is AND'ed with the FAST CLK signal by U9D and the output (Pin 11) is the clock signal X SMPL CTR CLK. It is used by the sample enable counter to count the number of data bits in the selected format and can be monitored at test point TP1. It is one half a fast clock wide (3 microseconds) and delayed also by one half fast clock period from X SP CLK TM. The timing signal X SP CLK is X SMPL CTR CLK gated by the NAND gate U9C to generate pulses only when data bias (including start bit) are present on the incoming data line, or when the control signal X DA SMPL EN is true (HIGH). This signal can be monitored at the test point TP3 and is illustrated in the timing diagrams (Figures A -60, A -66).

(3) XMTR 7 Sample Time Counter. - The purpose of this block is to divide each transmitter bit time into fast clock period, time elements (6 microseonds). The block consists of three counters U4, U5 and U6 (Figure A-18) connected to form a 12-bit synchronous counter. The counter is reset

to zero by the timing signal X N CLK, once per transmitter bit time--at the center of each bit. See Figure A-59. The counter is permanently enabled and clocked by the fast clock signal FAST CLK. The total count accumulation (12-Bit parallel word) is connected directly to the 12-bit digital comparator making up XMTR 8.

(4) XMTR 8 Sample Comparator. - This block compares the 12-bit count of the Sample Time Counter XMTR 7 and the Reference Time Counter XMTR 9. If they are equal, it generates the timing signal X SP CLK TM. If, at the center of transmitter bit time, the reference counter has more counts than the sample counter, the timing signal X SP CLK TM is also generated. The block consists of three 4-bit comparators U11, U12, and U13 (Figure A-10); two inverters U2E and U2F (Figure A-1); NAND gate U1D (Figure A-2); and NOR gate U1C (Figure A-2).

(a) The three 4-bit comparators are cascaded to form a 12-bit comparator for the outputs of the two counters. The equals output (Pin 3) of U13, which is HIGH when both counters are set to the same count, is inverted by U2F and logically OR'ed to the second output condition of the comparator block by the negative logic NOR gate U1C. Its output, Pin 8, is the signal X SP CLK TM.

(b) The A greater than B output (Pin 13) of U13 is logically AND'ed with the timing signal X N CLK (generated from X N CLK by the inverter U2E) so that the X SP CLK TM output signal is generated if the reference time counter has more counts than the sample time counter at X N CLK time. This sequence can be followed on the logic diagram (Figure A -53). It should be remembered that the reset for the Sample Time Counter and the Reference Time Counter is synchronous and therefore requires a clock pulse in addition to an active (LOW) at reset Pin 1 to accomplish the reset. The output signal X SP CLK TM is active (HIGH) for one period of the fast clock (6 microseconds).

(5) XMTR 9 Reference Time Counter. - This block determines the number of fast clock periods (6 microsecond increments) between the start of each transmitter bit and the start of each data bit. The input data to the transmitter need not be synchronous and may have a delay of two bit times.

(a) In start-stop modes this timing is automatically measured--the reference counter being reset at the beginning of each transmitter bit time--and disabled when the start bit is detected, for the remainder of the character. So the number of counts held in the reference counter is a measure of the phase difference and is used to generate a correctly phased serial-to-parallel clock. In the bit stream mode no start pulses are transmitted; the phase delay to be measured with an oscilloscope and manually set into the Center Sampling Adjustment switches. Hence, in this mode the reference counter is

permanently loaded with this manually entered count, which generates a correctly phased serial-to-parallel clock.

(b) The block consists of three counters U18, U19 and U20 (Figure A-18); two inverters U1A (Figure A-2), U17B (Figure A-l); a NAND gate U10B (Figure A-4); and a NOR gate U16B (Figure A-2). The three counters are cascaded to form a 12-bit synchronous counter, which is clocked by the fast clock signal FAST CLK. The mode of operation--automatic for star t-s top and manual for bit stream--is determined by the control signal BIT STREAM; when true (LOW), it forces a constant load (Pin 9) on all counters U18, U19 and U20 and disables the reset NAND gate U10B. Thus, in the bit stream mode the reference time counter is constantly loaded with the signals SMPL AD] 0 through SMPL AD] 11, which are manually preset with the Center Sampling Adjustment Switch. The pull-up resistors (R12, R13, R14) for the Sampling Adjustment Switch are located in circuit board assembly A2A2.

(c) In start-stop modes the control signal BIT STREAM is false (HIGH); if the X ST BIT DET and X DA SMPL EN are both HIGH (that is, at the beginning of a new character) the NAND gate U10B is enabled. The reference time counter is reset (zero count) at the beginning of each transmitter bit time by the timing signal X P CLK, which is derived from X P CLK by the inverter U1A. The counter is enabled to count by the output of U17B (Pin 4), which is HIGH at the beginning of each character. When a start bit is detected, the signal X ST BIT DET goes true (LOW). Through negative NOR gate U16B and inverter U17B this inhibits the counter and disables NAND gate U10B. One fast clock later the sample enable block becomes active and generates the signal X DA SMPL EN, which holds the count in the reference time counter for the duration of the character (that is: 6, 7, 8, or 9 bit times, depending upon selected format) l Thus the number of fast clock periods between the beginning of the transmitter bit time and the beginning of the data start bit is automatically counted into the reference time counter for every data character received, and the sample comparator block (XMTR 8) is able to determine the correct time for the serial-to-parallel clock.

(6) XMTR 10 Sample Enable. - The purpose of this block is to generate the control signal X DA SMPL EN, which is true (HIGH) for the number of transmitter bit times in the selected data input format. In start-stop modes the start bit is considered part of the incoming data code and is sampled in the same way as the data bits, but the stop bits are omitted.

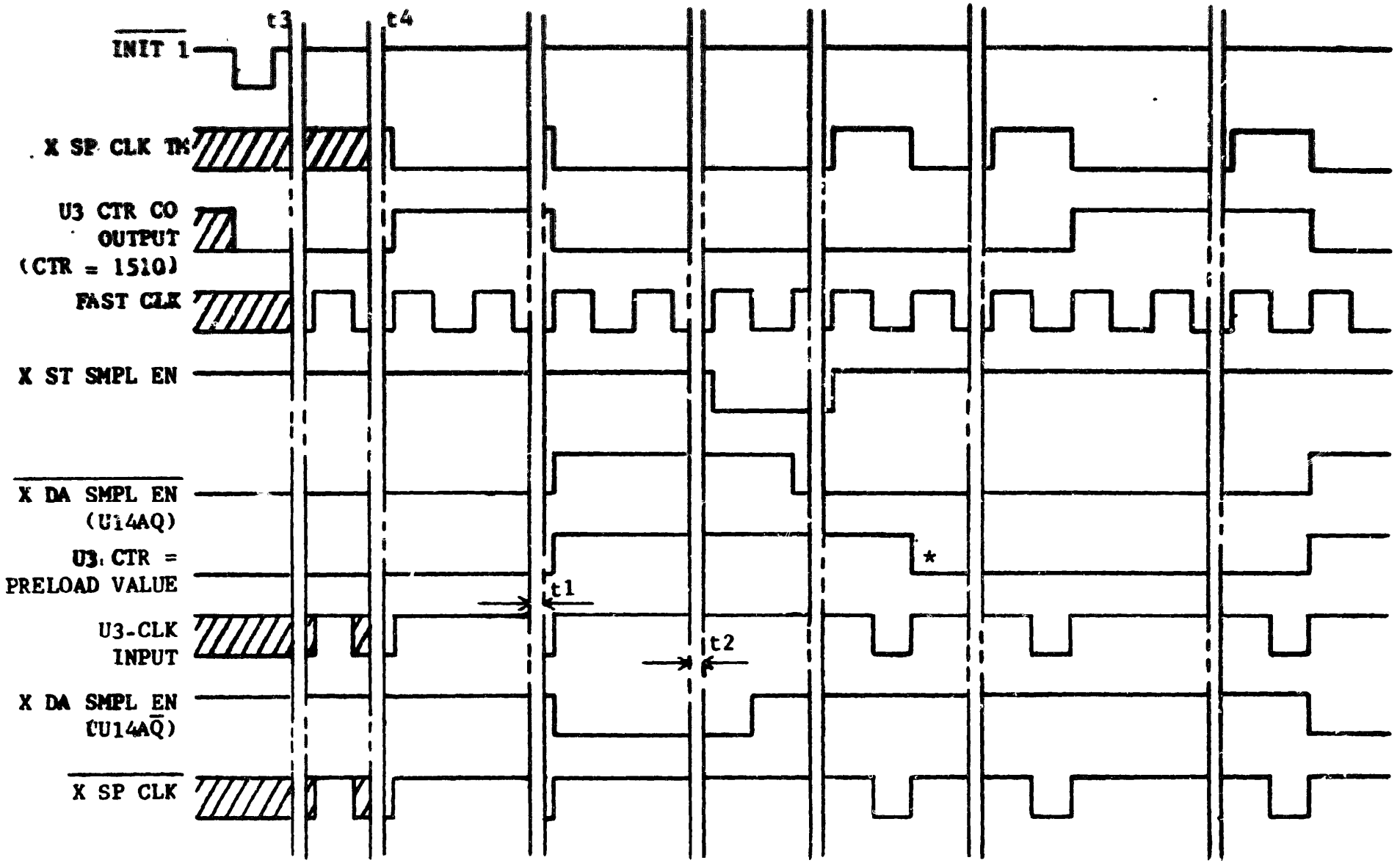
(a) The block consists of a 4-Bit counter U3 (Figure A-18); a J-K flip-flop U14A (Figure A-16); two NAND gates U1B, U16C (Figure A-2); and three inverters U2A, U2C, and U2D (Figure A-1). Upon initialization the counter U3 is directly reset to zero count, and the enable flip-flop U14A is reset, by the initialization signal $\overline{\text{INIT 1}}$. X DA SMPL EN is true (HIGH) at

this time. The sample bit counter U3 is enabled to count by enable signal X DA SMPL EN on Pins 7 and 10; it counts transmitter bit times X SP CLK TM signal time. When the count reaches 15, the carry output (Pin 15) is HIGH; it is inverted by the inverter U2C to generate the signal SMPL CTR LD. When true (LOW), SMPL CTR LD causes a load to be applied to the counter U3 (Pin 9). The carry signal from U3 also enables NAND gate U1B. At the next X SP CLK TM dock time the LOW output of NAND gate U1B is inverted by U2A to provide a HIGH at the J input (Pin 1) of the sample enable flip-flop U14A. The next fast clock signal sets U14A, forcing X DA SMPL EN false (LOW), thus disabling the counter U3. The next clock pulse to the counter loads it with the control signals SMPL CTR 1, SMPL CTR 2, SMPL CTR 4, and SMPL CTR 8; which are generated by the DATA FORMAT switch decoder block (XMTR 34 on board assembly A2A5). The loaded signals have a truth table shown in Table 4-9. Referring to this table, in Bit stream and Five Bit Start-Stop modes the counter is loaded with a count of 10; and in 6, 7 and 8 bit start-stop modes the count loaded is 9, 8, and 7, respectively. Both the inputs J (Pin 1) and K (Pin 4) of flip-flop U14A are LOW, hence the flip-flop cannot toggle and the counter remains disabled, holding the count previously loaded. The sample enable logic is enabled by the control signal X IN DA INH, which enables NAND gate U16C (Pin 9) when false (HIGH). When the start signal X ST SMPL EN from the start pulse detector (XMTR 5) becomes true (HIGH), the I< input (Pin 4) of flip-flop U14A is made HIGH via inverter U2D; the next fast clock resets flip-flop U14A making X DA SMPL EN true (HIGH), and enables the counter U3.

(b) The next X SMPL CTR CLK clock signal--appearing at center bit time--increments the counter and sets flip-flop U14A on the sixteenth count. Remember: the starting count depends upon the format selected, as shown in Table 4-9. The timing relationships are illustrated in Figure 4-1 Sample Enable Logic Timing Diagram. The signal SMPL CTR LD, which is LOW for one fast clock period (6 microseconds) to load the counter U3, can be monitored at test point TP2. The output signal X DA SMPL EN, which is LOW for the number of data bits in each character, can be monitored at test point TP7.

Table 4-9. Sample Enable Counter Load

MODE	SMPL CTR 1	SMPL CTR 2	SMPL CTR 4	SMPL CTR 8
BIT STREAM	LOW	HIGH	LOW	HIGH
5 BIT S-S	LOW	HIGH	LOW	HIGH
6 BIT S-S	HIGH	LOW	LOW	HIGH
7 BIT S-S	LOW	LOW	LOW	HIGH
8 BIT S-S	HIGH	HIGH	HIGH	LOW



t1 - time until 16th U3 CLK input increment

t2 - indeterminate time until (Memory Write complete)

*CTR = Preload count +1

t3 - indeterminant time until 1st FC leading edge after INIT 1 goes high

t4 - indeterminant time until U3 CTR CO goes high

Figure 4-1. Sample Enable Logic Timing Diagram

(7) XMTR 11 Clock Step Inhibit. - This block inhibits the transmitter step clock and sample enable logic if the system is in an ARQ or SYNC cycle, or if an inhibit supervisor is being transmitted or received. The block consists of a NOR gate U15A (Figure A-6) and two inverters U17A and U17F (Figure A-1). The control signals X ARQ INH, X SYNCING, X DA INH RCVD, and the inverted INH SUP INH are logically OR'ed in negative logic NOR gate U15A and inverted in U17F to produce the output signal X IN DA INH, which is used to inhibit the transmitter step clock.

c. A2A2 Fast Clock Step Generator (Logic Diagram Figure A-41, Block Diagram Figure A-30, Wiring Diagram Figure A-68, Timing Diagrams Figure A-59 thru A-64).

(1) XMTR 12 Fast Clock Generator. - This block generates a crystal controlled timing signal with a frequency of 153.6 kHz. The block consists of four inverters U1A, U4A, U4B and U4D (Figure A-2). Contral crystal Y1; four resistors R3, R5, R6, and R7; and capacitor C4. The oscillator consists of the crystal and inverters U48 and U4A, which are used as drivers. The resistor values are chosen to give a 50% mark-space relationship; some distortion may be encountered without causing a fault. The output of the oscillator is double-buffered by U4D and U1A; the output signal FAST CLK can be monitored at test point TP4. The frequency of the fast clock is 16 times the highest baud rate for the system and has a period of approximately 6 microseconds.

(2) XMTR 13 Initialize Logic. - This block generates the three initialization signals required by the system to initialize the memory and all logic elements in the transmitter. The block consists of two flip-flops U2A and U2B (Figure A-14); and two inverters U1B and U1C (Figure A-2). The power supply--on POWER UP or when the initialization button is pressed--generates the signal INIT 1, a 50 microsecond pulse occurring about 400 milliseconds after power is turned on or the button pressed. This signal is inverted by U1C to produce the initialization signal INIT 1. The first of three outputs of XMTR 13, it also performs important internal functions. It resets flip-flops U2A and U2B making both INIT 2 and INIT 3 active (LOW). When the first character (always an Inhibit Activate supervisory character) is written into the memory, Memory Write Pulse signal MEM WRITE A is generated. This clocks flip-flop U2B; its Q output (Pin 9) goes high disabling the INIT 3 signal. When the last character is written into the memory, the Memory Address signal MEM ADD MAX is generated. This clocks flip-flop U2A; its Q output (Pin 6) goes LOW disabling the INIT 2 signal through inverter (driver) U1B. The Memory Address signal MEM ADD MAX (LOW during the last memory address--one character time) can be monitored at test point TP2. Initialization signals INIT 2 and INIT 3 can be monitored at test points TP3 and TP1 respectively. The timing for the initializing sequence is shown in Figure 4-2. Figure A-53 describes the initialization sequence of the entire system.

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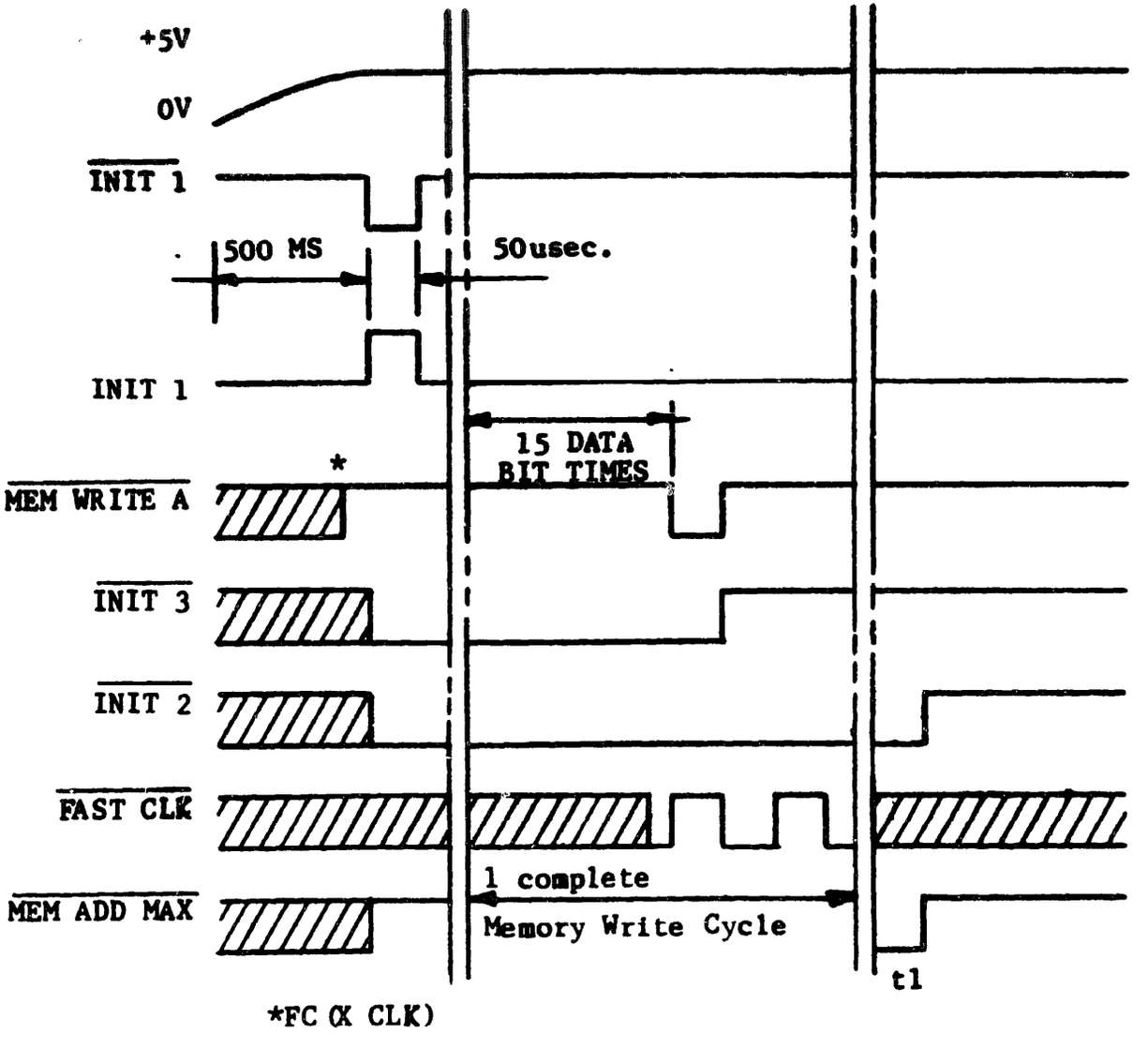


Figure 4-2. Initialize Logic Timing Diagram

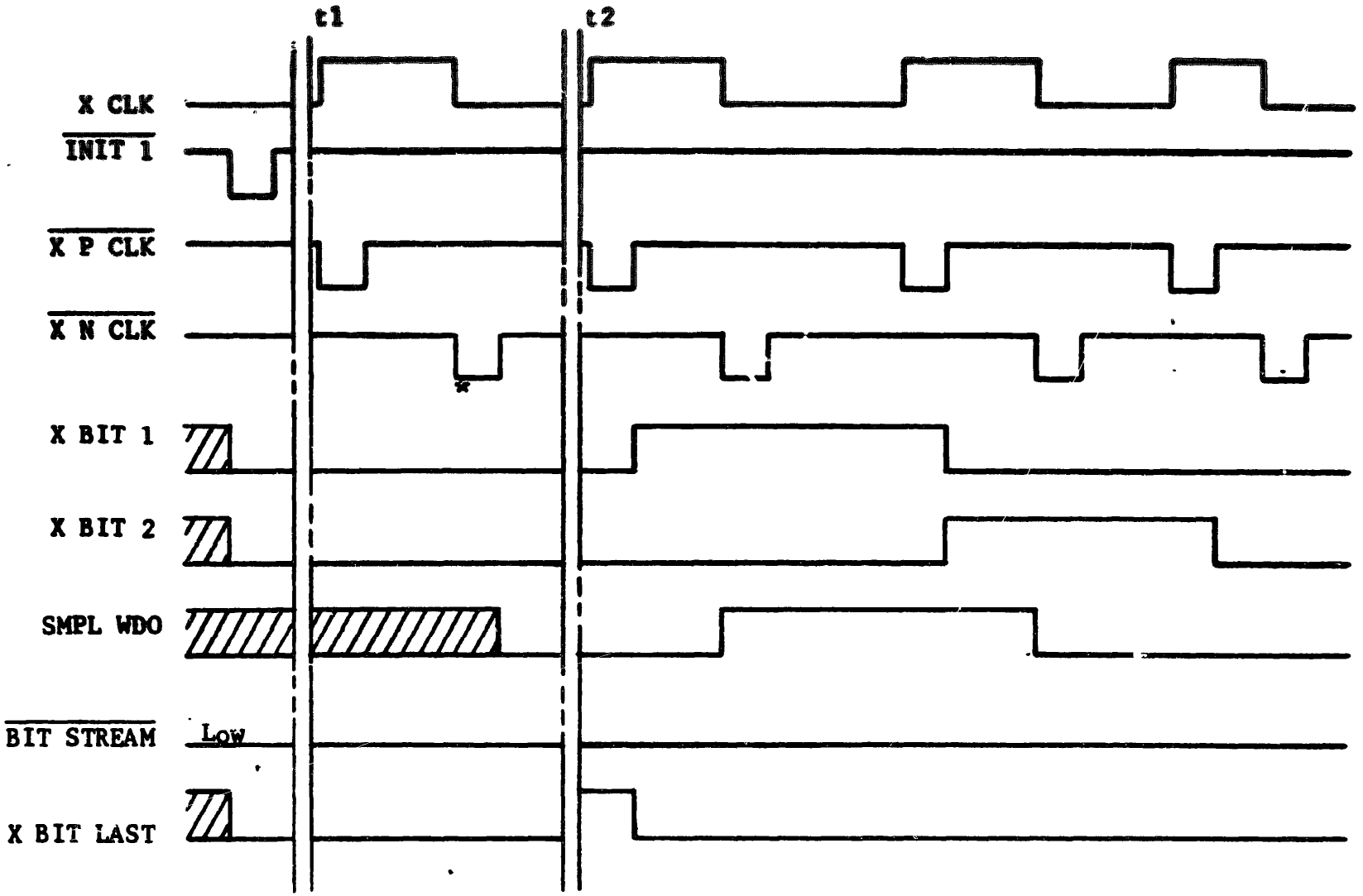
(3) XMTR 14 Data Window Logic. - The purpose of this block is to generate the sample window signal SMPL WDO for bit stream mode and start-stop modes. It determines when a new data character can be accepted by the transmitter logic. The block consists of a flip-flop U5A (Figure A-14); two NAND gates U7B, U7D (Figure A-2); two NOR gates U7A and U7C (Figure A-2); and three inverters U8B, U8E, U8F (Figure A-1).

(a) In bit stream format, when the control **BIT STREAM** is true (LOW), it disables NAND gate U7B, and enables NAND gate U7B through inverter U8B. The D input (Pin 2) of flip-flop U5A is HIGH only during the transmitter first bit time (timing signal X BIT 1). U5A is clocked every bit time by X N CLK. Its Q output (Pin 5) is enabled by NAND gate U7D and logically OR'ed to the start-stop version of the signal by negative logic NOR gate U7A. Therefore, in bit stream mode, output signal SMPL WDO is HIGH for one bit time at the start of each input data character.

(b) ln start-stop modes the control signal BIT STREAM is false (HIGH); NAND gate U7B is enabled and U7B is disabled. The first two transmitter bit time signals X BIT 1 and X BIT 2 are logically OR'ed in U7C via inverters U8F and U8E, then passed by the enabled NAND gate U7B to negative logic NOR gate U7A. Therefore, in all start-stop modes, output signal SMPL WDO is HIGH for the first two transmitter bit times. The output signal can be monitored at test point TP7; it is illustrated in Figure 4-3, Sample Window (Bit Stream Mode) and Figure 4-4, Sample Window (Start-Stop Mode).

(4) XMTR 15 XMTR Bit Counter. - The purpose of this block is to divide the transmitter character time into bit times, and to generate the control signals X BIT 1, X BIT 2, X BIT 3 and X BIT 6. The block consists of an 8-bit shift register U6 (Figure A-21), and two inverters U8D, U8C (Figure A-1). The shift register is reset to all O's by the initialization signal INIT 1. The transmitter last bit signal X BIT LAST is entered at the serial input (Pins 1 and 2). At the next transmitter bit time, this is shifted into QA (Pin 3) by the X P CLK signal and becomes output signal X BIT 1, At the next transmitter bit time it is again shifted into QB (Pin 4) and becomes output signal X BIT 2. At succeeding transmitter bit times shifts produce output signals sequentially. The last two signals, X BIT 3 and X BIT 6, are inverted by U8D and USC to produce X BIT 3 and X BIT 6. The timing of these signals is illustrated in Figure 4-5. X BIT 1 can be monitored at TP6, and X BIT 6 at TP5.

(5) XMTR 16 Last Bit Counter. - This block generates the transmitter last bit timing signal which occurs every eighth bit in bit stream and S-bit start-stop formats; and every eleventh bit in 6-, 7-, and 8-bit start-stop formats. This signal is the master character timing for the system because the receiver character timing is synchronized to the distant transmitter. The block consists of a 4-bit counter U3 (Figure A-18), and an inverter U8A

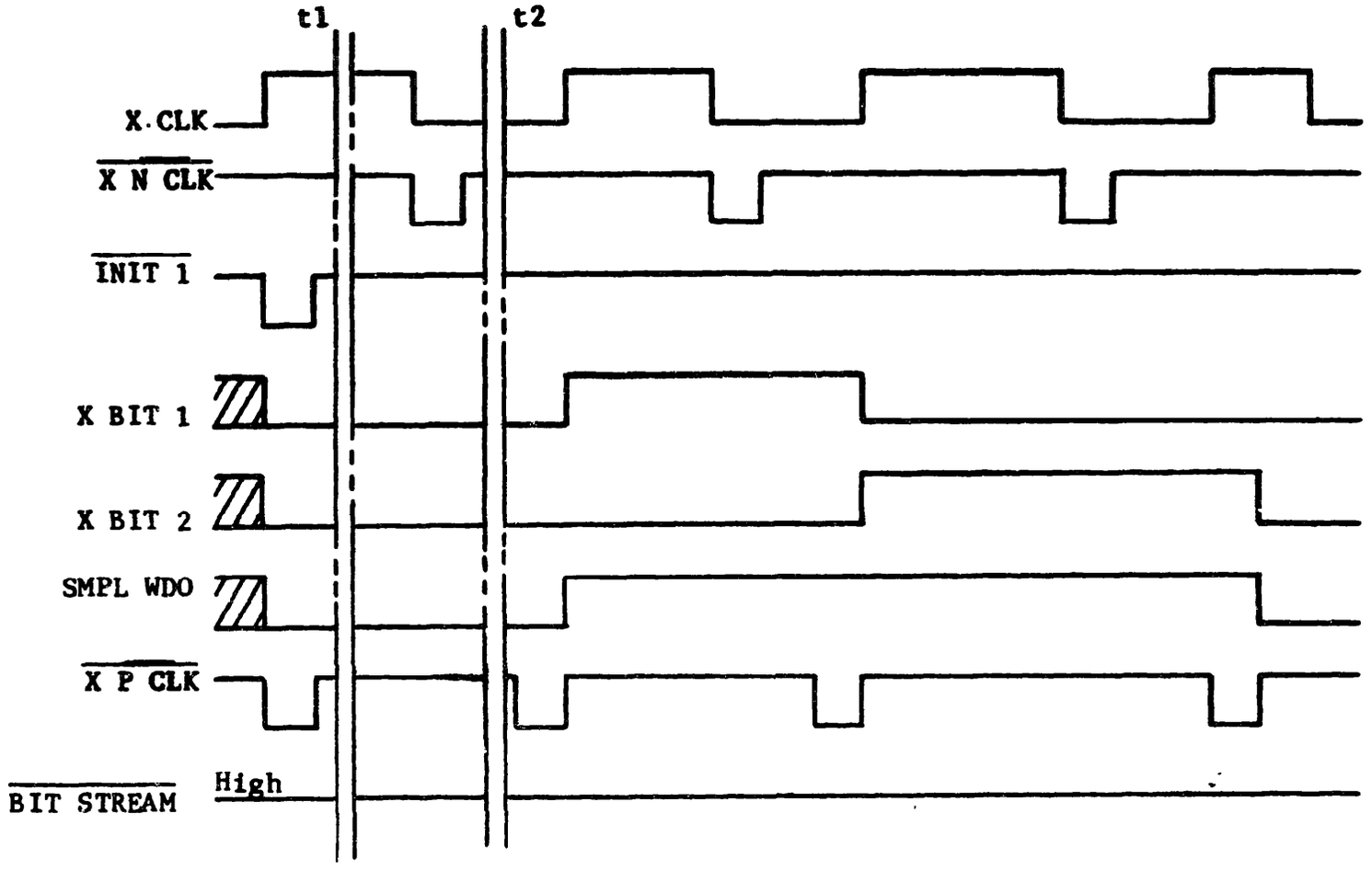


*1st X N CLK after $\overline{\text{INIT 1}}$ goes high

t1 - indeterminate time until X CLK goes high

t2 - indeterminate time from X Bit Last getting set high until next X CLK goes high

Figure 4-3. Sample Window - (Bit Stream Mode)



t1 = indeterminate time until X CLK goes Low
t2 = indeterminate time until X P CLK goes Low

Figure 4-4. Sample Window - (Start/Stop Mode) Timing Diagram

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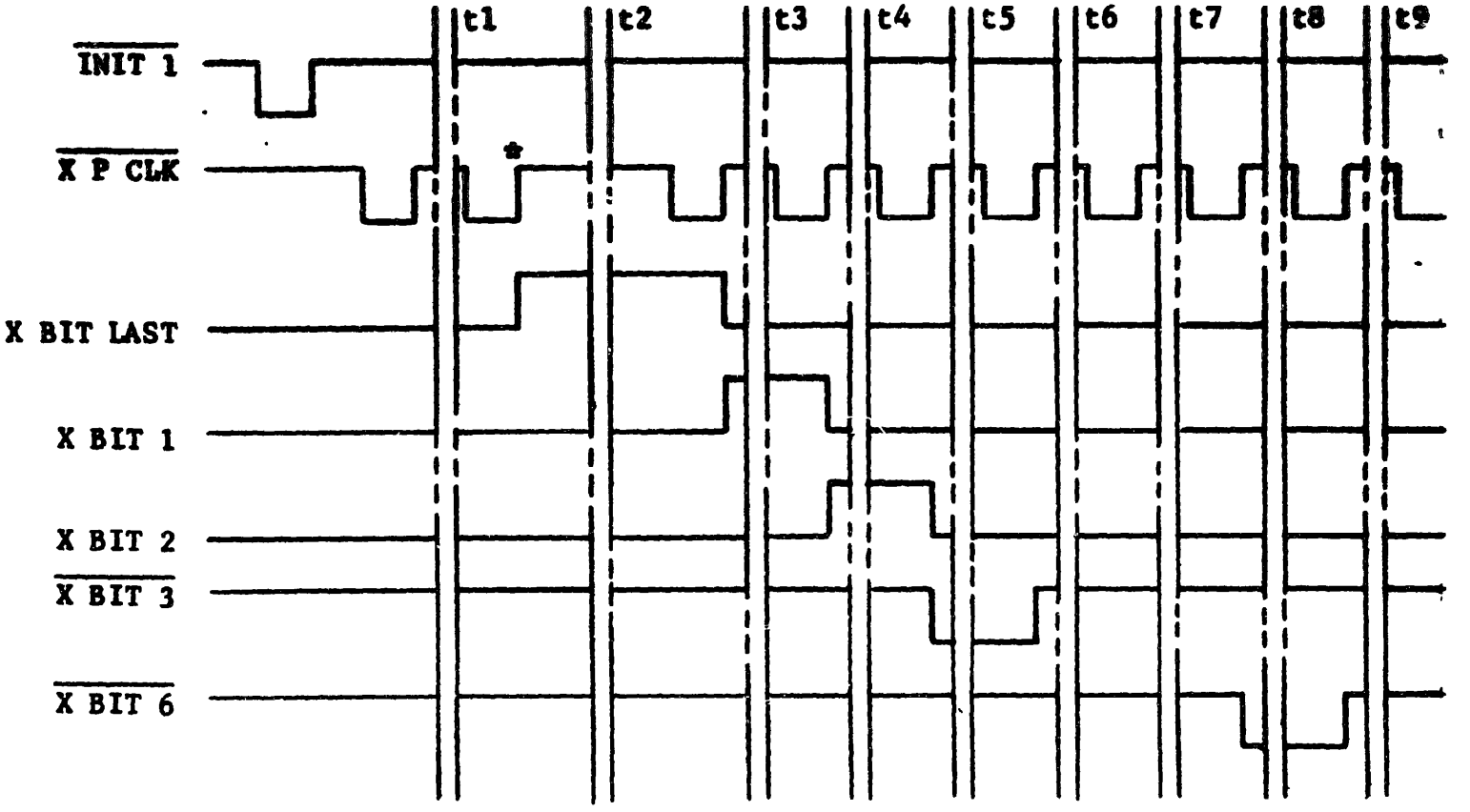


*15th $\overline{\text{X P CLK}}$

t1 - indeterminate time until 15th $\overline{\text{X P CLK}}$ goes low

t2 thru t9 - indeterminate time until $\overline{\text{X P CLK}}$ goes low

Figure 4-5. XMTR Bit Counter Timing Diagram

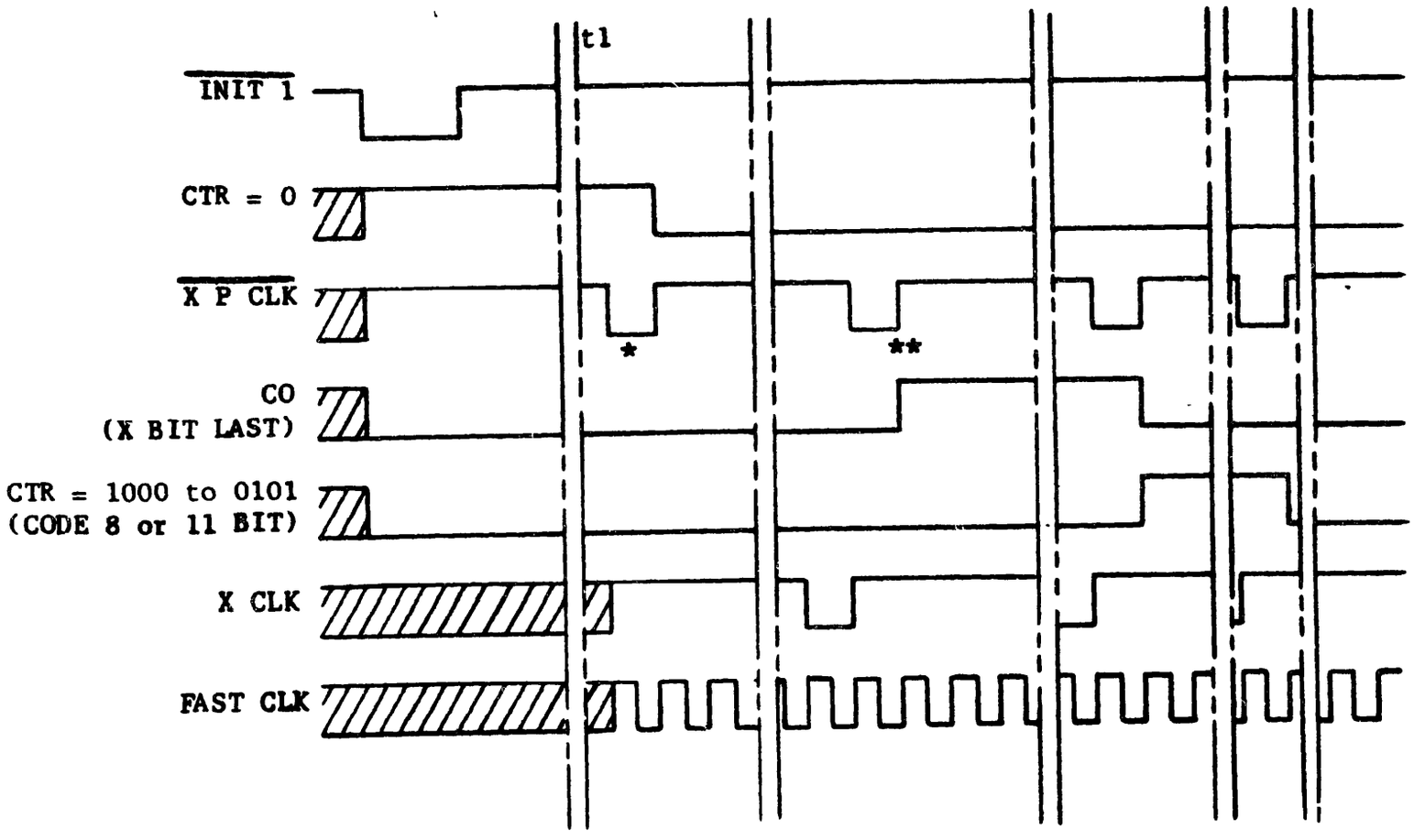
(Figure A-1). The counter is reset to all zero count by the initialization signal INIT 1, and is permanently enabled to count transmitter bit times. When a count of 15 is reached (maximum count), the carry output (Pin 15) is set HIGH and produces the output signal X BIT LAST. This is inverted by U8A producing the X BIT LAST output, and is also applied to the load input (Pin 9) of the counter so that on the next clock signal--X P CLK--the counter is loaded with eight (bit stream and 5-bit start-stop formats) and five (6-, 7-, and 8-bit start-stop formats). When the count again reaches 15 (maximum count) an X BIT LAST signal is again generated. This occurs every eighth bit or every eleventh bit depending upon selected format. The timing for this generator is illustrated in Figure 4-6 Last Bit Counter, and the signal X BIT LAST can be monitored at test point TP8. The control signals CODE 8 BIT and CODE 11 BIT are complementary, generated by the Format Switch Decode block (XMTR 34) on circuit board A2A5.

(6) XMTR 17 Bit 6A Generator. - The purpose of this block is to remove a glitch in the bit stream step clock. The block consists of a single flip-flop U5B (Figure A-16). It times the timing signal X BIT 6 to the transmitter clock X CLK 1 thereby generating the output signal X BIT 6A.. The timing is illustrated in Figure 4-7, XMTR Bit 6A Generator, and timing diagram in Figures A-59 through A-62.

d. A2A3 Inhibit Control XMTR Clock Generator (Logic Diagram Figure A-42, Block Diagram Figure A-31, Wiring Diagram Figure A -69, Timing Diagrams Figures A-59 through A-64.

(1) XMTR 18 XMTR Clock Generator. - This block generates the timing signals X P CLK and X N CLK (negative-going pulses of 6 microseconds duration) at the rise and fall of the transmitter clock signal X CLK-1. The block consists of two flip-flops U21A, U21B (Figure A -14); two NAND gates U20B, U20C (Figure A-2); and five inverters U13A, U13B, U13C (Figure A-l) U12A and U12B (Figure A-2).

(a) The two flip-flops, U21A and U21B, form a 2-bit shift register that is continually clocked by the fast clock signal FAST CLK. The transmitter clock signal X CLK is inverted by the U13C to generate X CLK-1, which becomes the input to the 2-bit shift register and is shifted into the flip flops U21A and U21B by sequential fast clock pulses. Consider the transmitter clock X CLK-1 to be LOW; after two fast clock periods, the output Q terminals of both flip-flops are also LOW, and the Q terminals HIGH. Referring to the logic diagram Figure A-42, both NAND gates, U20B and U20C, are disabled yielding HIGH outputs. When the transmitter clock signal X CLK-1 goes HIGH, the first fast clock toggles U21A; its Q output (Pin 5) goes HIGH enabling NAND gate U20C. Its output (Pin 8) goes LOW generating the signal X P CLK. At the next fast clock (6 microseconds later) the second flip-flop U21B toggles, its Q output (Pin 8) goes LOW disabling U20C. Its output



*1st X P CLK after $\overline{\text{INIT 1}}$

**15th X P CLK after $\overline{\text{INIT 1}}$

= Indefinite Logic State or Don't Care

t1 - indeterminate time until 1st X P CLK goes low

Figure 4-6. Last Bit Counter Timing Diagram.

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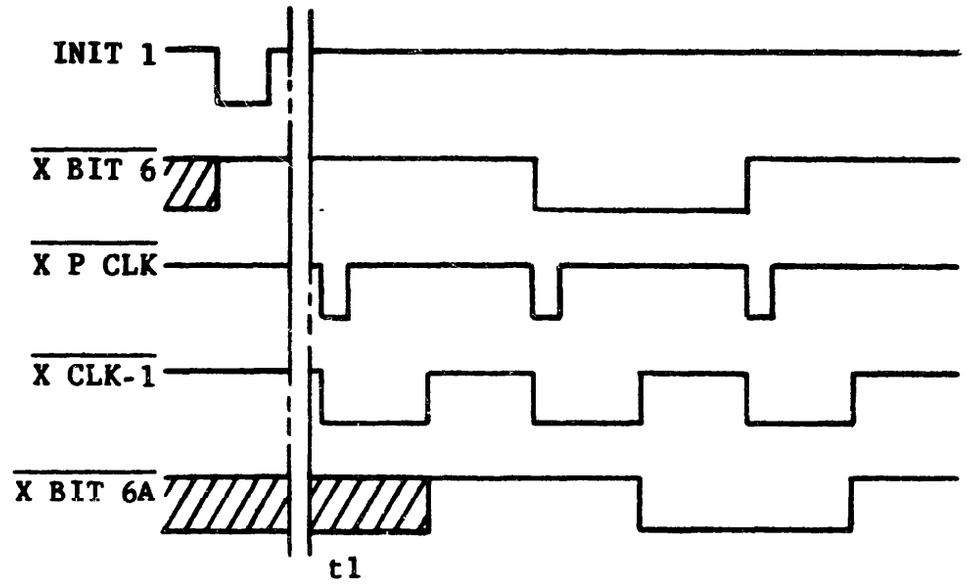


t1 - indeterminate time until $\overline{\text{X CLK-1}}$ goes low

Figure 4-7. XMTR Bit 6A Gen Timing Diagram.

returns to the HIGH condition, completing the generation of the six microsecond pulse.

(b) The reader should follow the logic diagram to see that a similar pulse is generated at the output (Pin 6) of the NAND gate U20B when the transmitter clock signal X CLK 1 falls from a HIGH to a LOW level, which generates the output signal X N CLK. The signals are inverted by U13A and U13B to provide timing signals X P CLK and X N CLK; and again inverted and buffered by drivers U12B and U12A to produce the output timing signals X P CLK and X N CLK. The latter can be monitored at test points TP4 and TP6 respectively. The timing for the above signals is illustrated in the timing diagrams Figures A-59 and A-62.

(2) XMTR 19 XMTR Last Clock Generator. - This block generates the timing signals X N L CLK and X P L CLK and their complements--three microsecond timing pulses that occur once per character. The block consists of a flip-flop U14A (Figure A-14); two NAND gates U5B, U5C (Figure A-4); and four inverters U6A, U6B, U6C, U6D (Figure A-2). Flip-flop delays the X P CLK signal by one fast clock period (6 microseconds); Q output (Pin 5) is applied to NAND gate U5 (Pin 3). The gate is enabled by the transmitter bit signal X BIT 1 (Pin 5) and the fast clock signal FAST CLK (Pin 4). Thus the output of U5B (Pin 6) goes LOW for the second half of the fast clock period during the first transmitter bit and at the delayed X P CLK time, to generate the signal X PL CLK. The timing is illustrated in Figure 4-8 The X N CLK signal is applied to input (Pin 9) of NAND gate USC, which is enabled by the transmitter bit signal X BIT LAST (Pin 11) and the fast clock signal FAST CLK (Pin 10). Thus the output of USC (Pin 8) goes LOW for the second half of the fast clock period during the last transmitter bit and at X N CLK time, to generate the signal X NL CLK. The two signals are inverted by U6A and U6D to generate the output signals X PL CLK and X NL CLK, and inverted again by U6B and U6C to produce the buffered output signals X PL CLK and $\overline{\text{X NL}}$ CLK. They can be monitored at test points TP2 and TP6 respectively.

(3) XMTR 20 Clock Step Generator. - The purpose of this block is to generate the transmitter step clock signal X CLK ST, which requests a new character or data bit from the data source. The block consists of a flip-flop U8B (Figure A-16); four NAND gates U17C; U17D (Figure A-3), U4B (Figure A-2), and U11A (Figure A-4); and a NOR gate U4D (Figure A-2).

(a) In the bit stream mode, the transmitter clock step consists of six periods of the transmitter clock signal X CLK 1 (see Figure 4-9). Mode control signal BIT STREAM (LOW) disables NAND gate U4B but enables the negative logic NAND gate U17C so that its output (Pin 10)) is the transmitter clock signal X CLK 1. This is connected to input (Pin 11) of NAND gate U17D, which is enabled by the clock step enable signal CLK ST EN. The J-K flip-flop U3B is clocked by the transmitter clock signal X CLK 1 and is reset

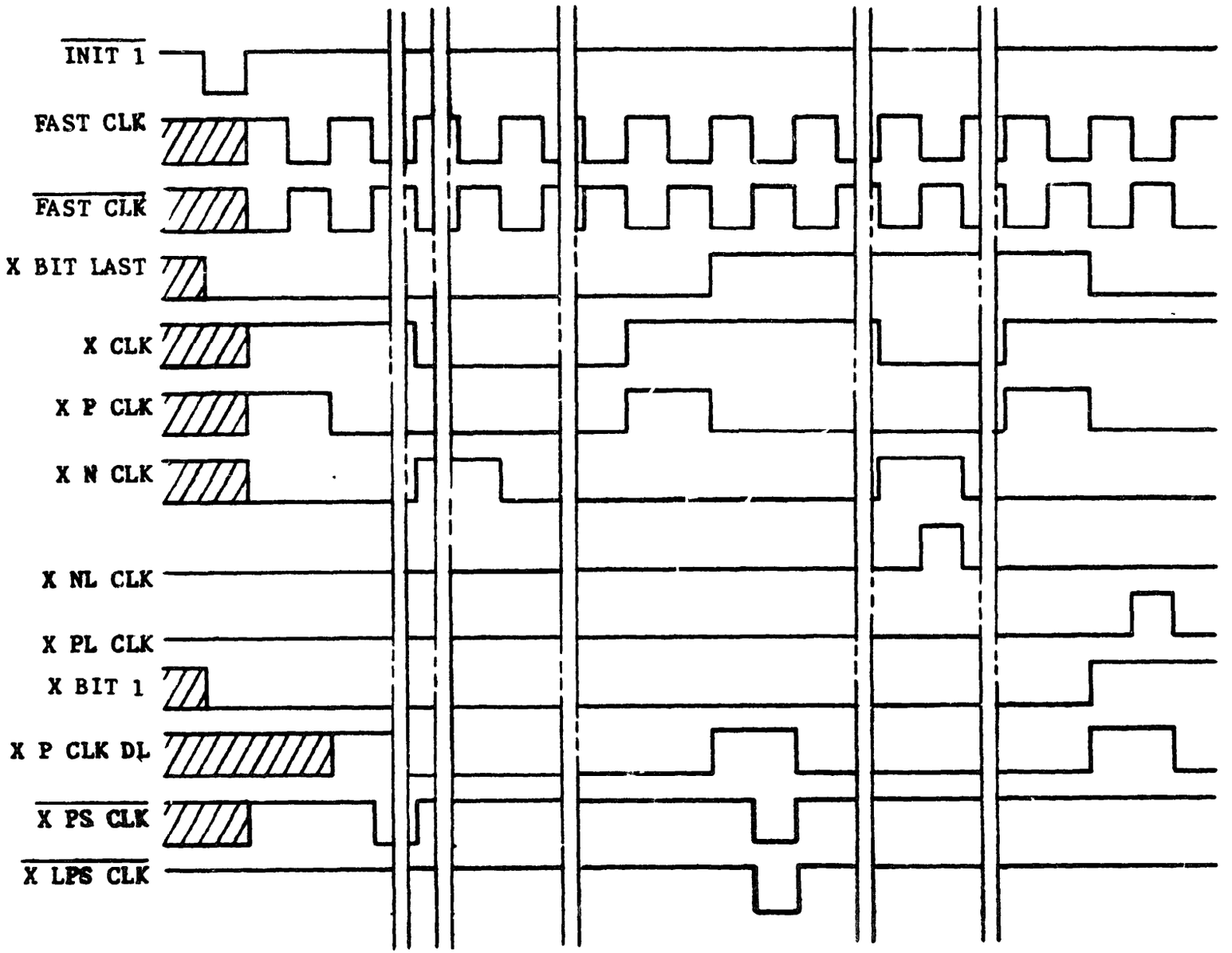
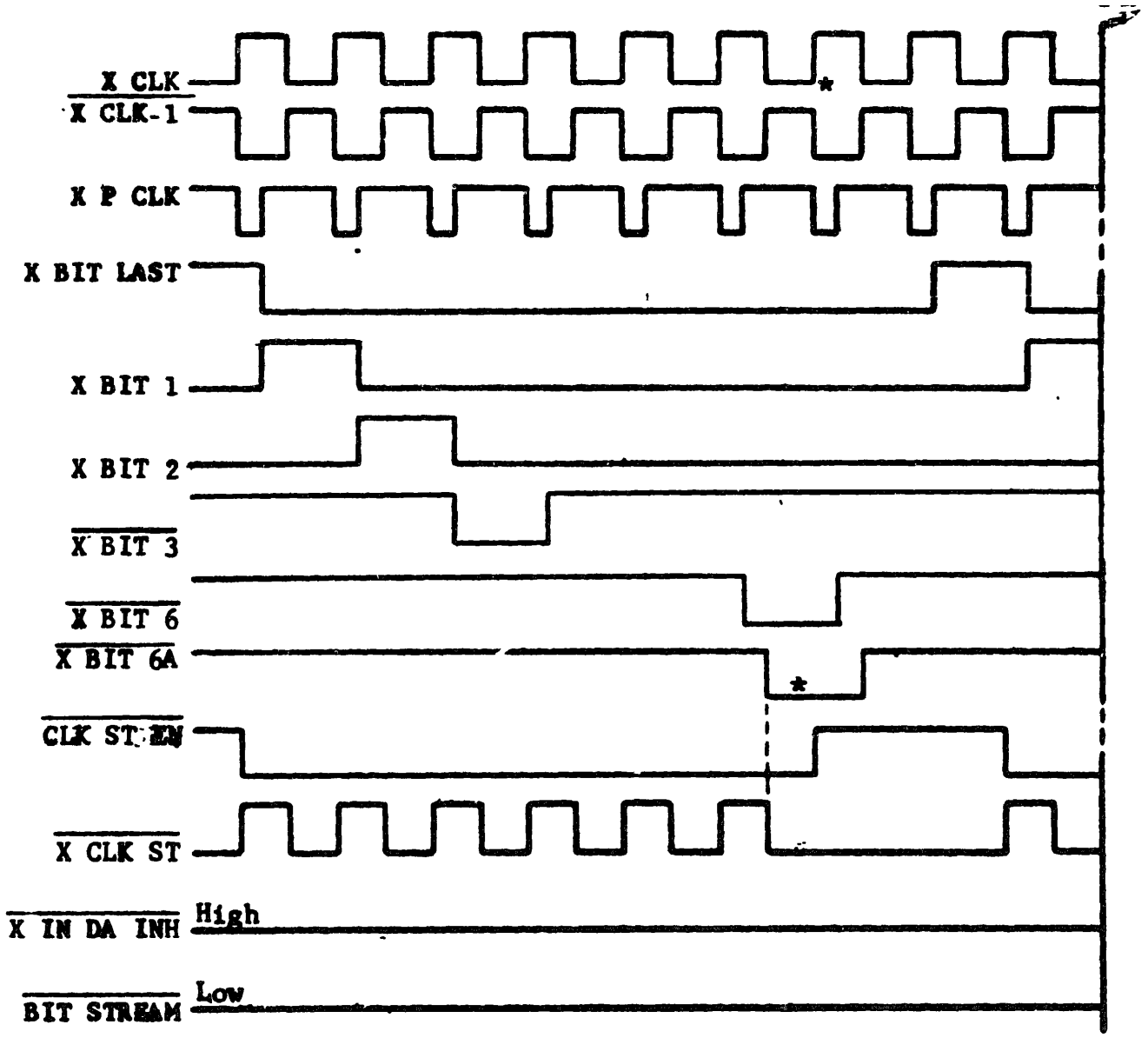


Figure 4-8. Clock Generator Timing Diagram.



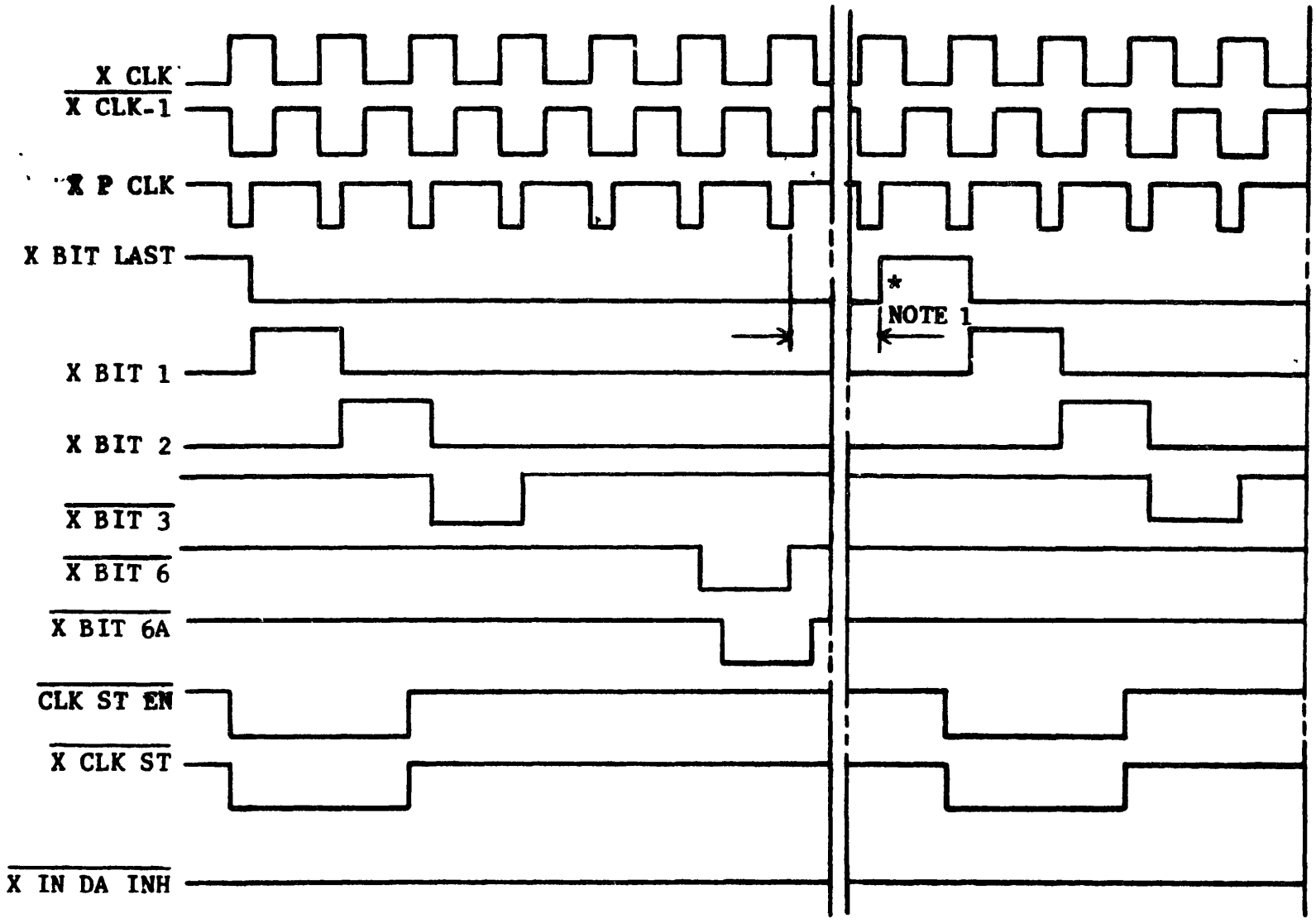
*Prevents spike on $\overline{\text{X CL ST}}$ line when FF U3B$\bar{Q}$ is going high and X CLK is going high

Figure 4-9. Clock Step Generator - Bit Stream Mode Timing Diagram.

when the control signal X IN DA INH is true (LOW), which disables the transmitter step clock in all modes.. The transmitter bit signal X BIT LAST is applied to the J input (Pin 8) of flip-flop U3B; at the next transmitter clock signal X CLK 1 (which occurs at the beginning of a new character) the flip-flop is set; output Q (Pin 6) goes LOW, to produce the signal CLK ST EN, which enables the negative logic NAND gate U17D. The output of the gate (Pin 13) is the transmitter clock signal. It is inverted by enabled NAND gate U11A to become the transmitter step clock signal X CLK ST. The transmitter bit signal X BIT 6 is connected via the negative logic NOR gate U4C to the K input (Pin 11) of flip-flop U3B; thus after six bit times the flip-flop is reset disabling NAND gate U17D and holding the step clock signal X CLK ST (HIGH). NAND gate U11A is disabled by the timing signal X BIT 6A to prevent a switching glitch when flip-flop U3B changes state. In bit stream the transmitter step clock is six periods of the transmitter clock followed by two blank periods. The waveform can be monitored at test point TP3; it is illustrated in Figure 4-9.

(b) In start-stop formats the transmitter step clock signal X CLK ST is active (LOW) for the first two transmitter bit times. The mode control signal BIT STREAM (HIGH) enables NAND gate U4B and disables NAND gate U17C, which permanently enables NAND gate U17D. Hence when the flip-flop U3B is set at the end of the transmitter last bit time, it generates the clock signal X CLK ST directly. NAND gate U6B is now enabled and, se the trailsmitter bit signal, X BIT 2 is applied to the K input (Pin 11) of flip-flop U3B via U4B and U4C. This causes the flip-flop to reset after two transmitter bit times; the transmitter bit signals X BIT 6 and X BIT 6A have no effect in these modes. Thus in all start-stop modes the transmitter step clock signal X ST CLK is LOW for the first two transmitter bit times and HIGH for the remainder of the character. The waveform is illustrated in Figure 4-10; It can be monitored at test point TP3. It should be remembered that the final transmitter step clock is inverted by the line driver (XMTR 46) on circuit board A2A8.

(4) XMTR 21 Parallel-To-Serial Clock Generator. - This block generates the clock signal that converts the parallel data into serial data for transmission. (This clock is not equally spaced; more time is required at the last bit time for data handling, hence the final serial data output is retimed to the transmitter clock signal X CLK 1). The block consists of a flip flop U14B (Figure A-14); three NAND gates U4B, U19C, and U19D (Figure A-2); a NOR gate U19B (Figure A-2); and an inverter U10C (Figure A-1). At all transmitter bit times except the last NAND gate U4B is enabled by the signal X BIT LAST being false (HIGH); thus its output (Pin 3) is the timing signal X P CLK DL, which occurs once per bit time. This is passed via NOR gate U19B and gated by the fast clock signal FAST CLK in NAND gate U19D. Hence for all bit times except the last the parallel-to-serial clock is the last half of the X P CLK DL signal; it occurs one fast clock period



*NOTE 1 1 Clock period for 5 Bit Code (Code 8 Bit Line high)

4 Clock periods for 6,7,8 Bit Codes (Code 11 Bit Line high)

Figure 4-10. Clock Step Generator - start/Stop Mode Timing Diagram.

(6 microseconds) after the X P CLK signal. During the last transmitter bit time this block waits until the end of the memory write pulse MEM WRITE A (applied to the D input (Pin 12) of flip-flop U14B), and is then clocked by the fast clock signal FAST CLK. The Q output at Pin 9 is passed via NOR gate U19B, then gated by the fast clock signal FAST CLK in NAND gate U19D, which selects the second half of the signal so that the last bit parallel-to-serial clock is at least 3 microseconds after the memory write pulse. The parallel-to-serial clock waveform is illustrated in Figure 4-11; it can be monitored at test point TP7. X PS CLK is inverted by the U10C, then AND'ed with the transmitter last bit signal X BIT LAST in U19C to produce X PS CLK, which is used for timing in the Memory counter (XMTR 39), Parity Checker (XMTR 43) and the Sync cycle control (XMTR 27).

(5) XMTR 22 Inhibit Received Control. - This block processes the receiver activate flag and--depending upon the strap option--halts the transmitter or just indicates that an Inhibit Activate supervisory character has been received. The block consists of three flip-flops U8A, U8B and U1A (Figure A-14); a NAND gate U9D (Figure A-2); a NOR gate U9A (Figure A-2); and inverter U2A (Figure A-1). A two-position plug is used to select the inhibit option. Flip-flop U1A and U8B are reset, and U8A is set, by the initialization signal INIT 2, which disables the inhibit logic during the initialization sequence. The inhibit activate flag from the receiver R INH ACT FLG is connected to the D input of flip-flop U8A, which is clocked at the end of the active character by the timing signal X N L CLK. If an active flag (HIGH) is received, the Q output (Pin 5) of U8A goes HIGH; it is retimed to the transmitter clock by flip-flop U8B and inverted in U2A to produce indicator signal R DIST INH IND. The front panel indicator is illuminated by R DlST INH IND FP via resistor R2. The NAND gate U9D is enabled by the initialization signal INIT 2 via the NOR gate U9A or when the inhibit option plug is set for OPTION A. When an activate inhibit activate flag is received Q output (Pin 5) of flip-flop U8A will generate the control signal X DA INH RCVD, via NAND gate U9D, to inhibit the transmitter step clock. About half a bit later the timing signal X PL CLK clocks flip-flop U1A, which generates the supervisory control signal INH GEN; the transmitter sends continually the inhibit supervisory character selected on the front panel or set remotely by the signal LOCAL INH L. The signal INH GEN can be monitored at test point TP1. The timing is illustrated in Figure 4-12.

(6) XMTR 23 Inhibit Request Control. - This block interrupts normal data transmission for one character in order to transmit an Inhibit Activate or Inhibit Deactivate supervisory character. The block consists of three flip-flops U18A, U18B (Figure A-17), U3A (Figure A-16); four NAND gates U17A, U17B (Figure A-3), and U11B, U11C (Figure A-4); five NOR gates U9B, U9C, U16A, U16C, U16D (Figure A-2); and six inverters U10A, U10E, U10F, U12C, U12D, U13D, (Figure A-1). The front panel INHIBIT ACTIVATE-DEACTIVATE switch signals $\overline{\text{FP INH ACT}}$ and FB INH DEACT are

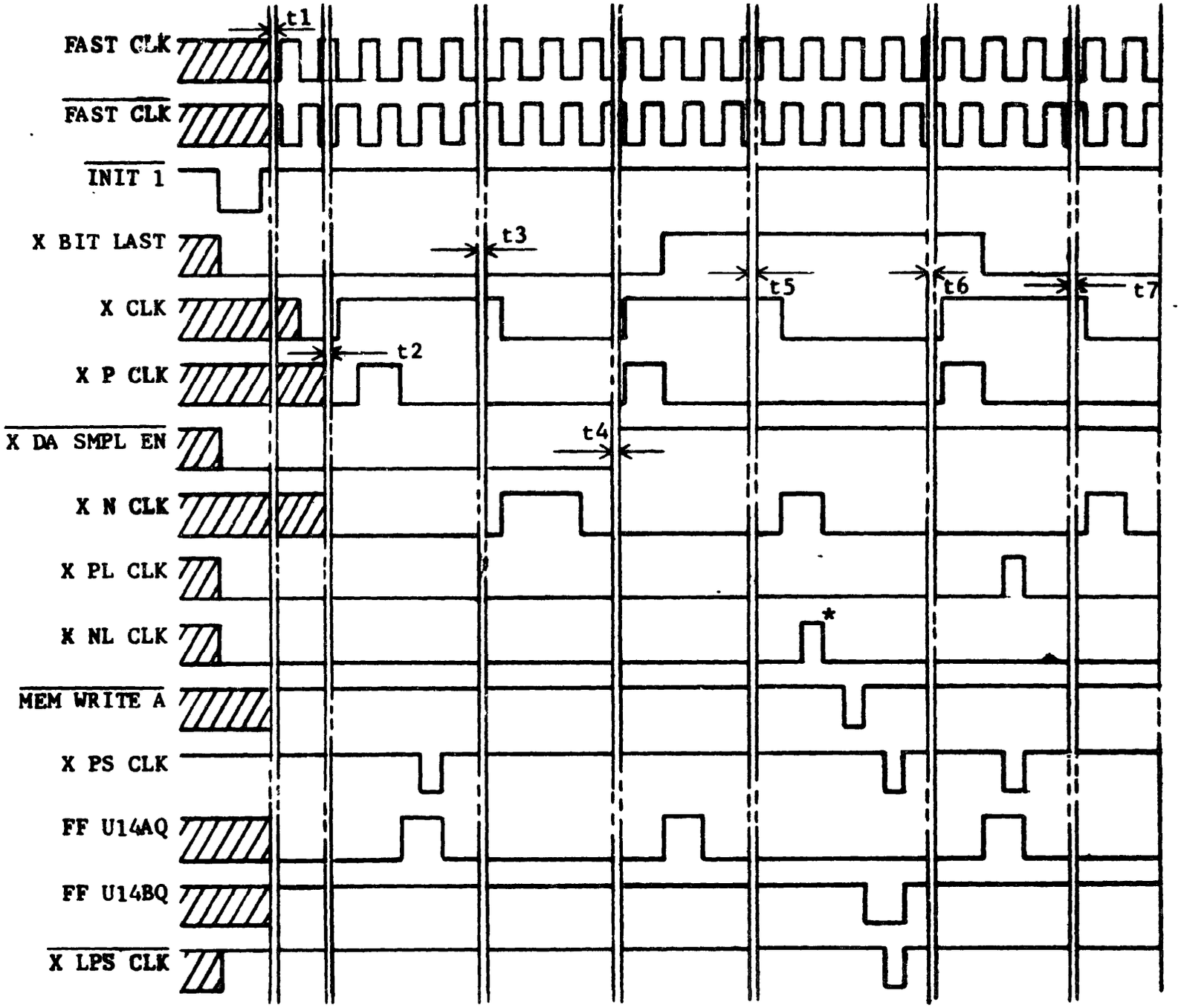
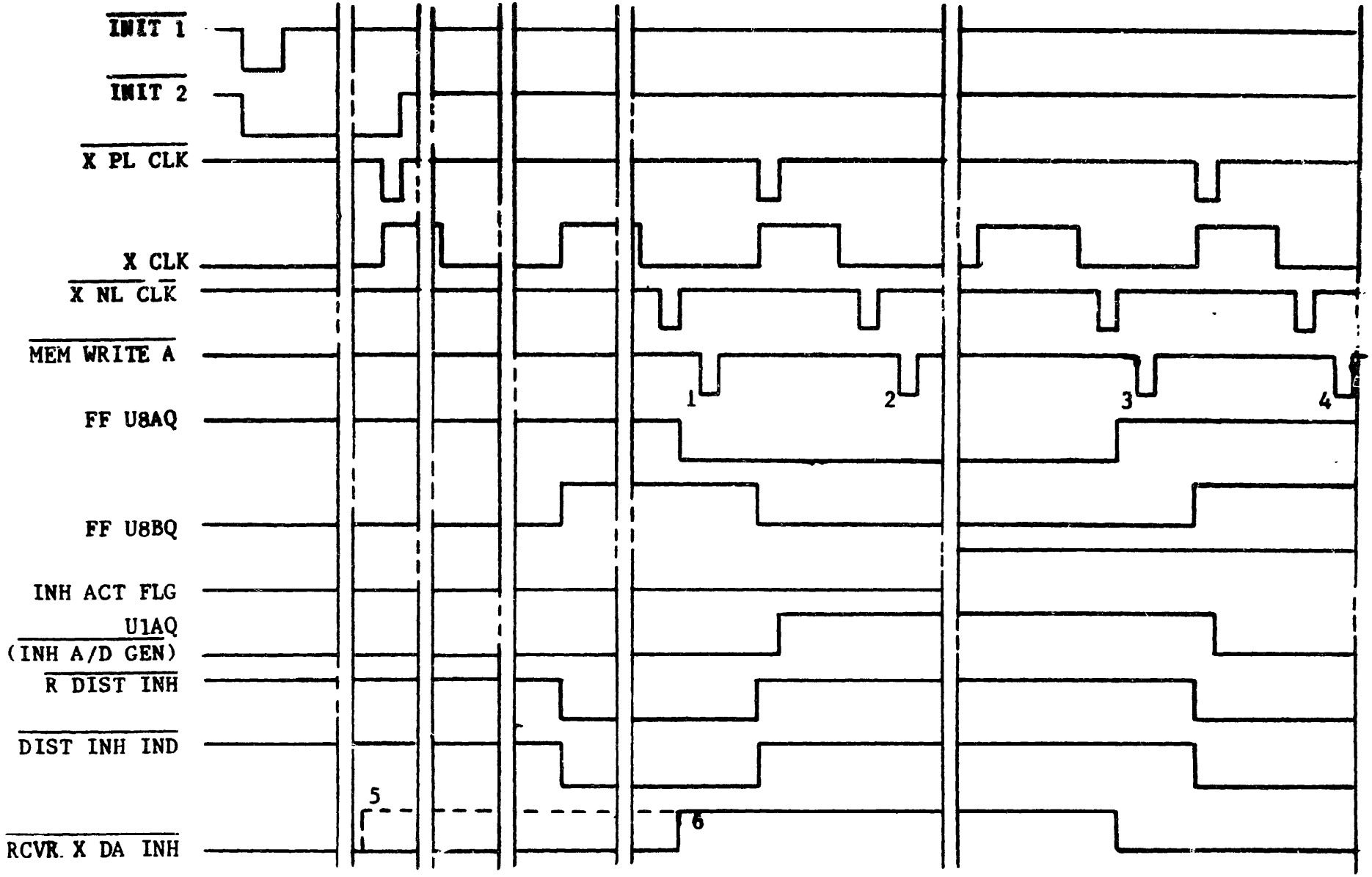


Figure 4-11. Memory Write Control and Parallel/Serial Clock Gen Timing Diagram..



1. Writes INH ACT character. 2. Write INH DEACT, DATA or IDLE (Refer to Inhibit Receiver Control Description). 3. Writes Last character. 4. Write INH ACT or INH DEACT character into Memory. 5. If Plug (P1) in R5 position. 6. If Plug (P1) in GND position

Figure 4-12. Inhibit Received Control Logic Timing Diagram

de-glitched by the RS flip-flop consisting of U9B and U9C, then logically OR'ed to the remote inhibit control signal LOCAL lNH by the negative logic NOR gate W16A --the output (Pin 3) of which goes from L0W to HIGH to generate the Inhibit Activate supervisory character. This is connected to the K input (Pin 1) of flip-flop WMA via the NAND gate U17A, and its complement to the J input (Pin 4) via NAND gate U17B. The NAND gates U17A and U17B inhibit the generation of inhibit supervisory characters if the system is in an ARQ or SYNC cycle. ControI signals X SYNCING and X ARQ INH are Iogitally OR'ed by NOR gate U16D, and enable the NAND gates U17A and U17B. Flip-flops U18A and U18B are preset and U3A is reset by the initialization signal INIT 2, which also inhibits the generation of either of the inhibit supervisory characters. The flip-flops areclocked at the end of each character by the timing signal X L PS CLK, derived from X L PS CLK by inverter U13D; they are connected as a 2-bit shift register.

(a) When the INHIBIT switch on the front panel is changed, or the remote LOCAL lNH signal changes state, flip-flop U18A changes state at the end of the active character, followed at the end of the next character by a change of state of U18B. Assume the switch is changed from the DEACTIVATE to the ACTIVATE position: initially both the flip-flops are reset, and the Q outputs (Pins 7 and 9) are LOW, disabling NAND gates U11B and U11C. The output signal SWITCH INH A/D is LOW indicating an Inhibit Deactivate supervisory character. When the switch change state at the end of the active character; the Q output (Pin 7) becomes HIGH enabling NAND gate U11B making its output (Pin 6) LOW. This is the signal INH ACT GEN. Negative logic NOR gate U16C produces control signal INH SUP INH (which holds the transmitter step clock). At the end of the next character flip-flop U18B is also set, its output Q (Pin 10) going LOW disabling both output signals.

(b) When the front panel INHIBIT switch is toggled to the DEACTlVATE position, the Inhibit Deactivate supervisory character is generated. In this case NAND gate U11C is enabled and the signals INH DEACT GEN and INH SUP INH are generated. Flip-flop U3A is used to remember the last inhibit supervisory character transmitted and to light the front panel indicator INHIBIT REQuest indicator. The supervisory generator signals INH ACT GEN and INH DEACT GEN are inverted by U10F and U10E and applied to the J input (Pin 1) and K input (Pin 4) of flip-flop U3A, which is clocked at the fall of the transmitter clock signal X CLK 1. The indicator light is driven from the Q output (Pin 3) via driver inverter U12D and resistor R1. Inverter U12C generates the inverted transmitter clock signal X CLK-1.

(7) XMTR 24 Memory Write Control. - This block generates the memory write pulse MEM WRITE A and its compliment MEM WRITE A. It consists of two flip-flops U7A and U7B (Figure A-14); two NOR gates U20A, U20D (Figure A-2); a NAND gate USA (Figure A-4); and an inverter U10B (Figure A-1). The two NOR gates U20A and U20D are connected as an R-S

flip-flop that is reset by the X P CLK signal and set by the X N CLK signal. The memory write inhibit signal MEM WRITE INH signal at U20D pin 11 is false (HIGH) between the X N L CLK time and the next X P CLK time, or about one half a bit time at the end of each character; when it is true (LOW), it holds the two flip-flops U7A and U7B reset. The Q output (Pin 5) of U7A inhibits NAND gate USA, preventing the generation of the memory write pulse The data sample enable signal X DA SMPL EN goes HIGH when the last data bit has been sampled; it is connected to the D input (Pin 2) of U7A. If the memory write inhibit signal MEM WRITE INH is false (HIGH), this is clocked into the Q output with the rise of the next fast clock signal FAST CLK 1. Thus the Q output (Pin 5) of U7A goes HIGH enabling NAND gate USA to generate the memory write signal MEM WRITE A for the second half of the fast clock, when the signal FAST CLK is also HIGH. The next rise of the fast clock signal FAST CLK sets the second flip-flop U7B and its Q output (Pin 8) goes LOW disabling NAND gate USA. The next X P CLK signal generates the reset signal MEM WRITE INH and resets both flip-flops (U7A and U7B) ready for the next character. The memory write signal MEM WRITE A is inverted by U10B to produce the complement, MEM WRITE A. The timing for these signals is illustrated in Figure 4-11.

e. A2A4 XMTR ARQ and SYNC Control (Logic Diagram Figure A-43, Block Diagram Figure A-32, Wiring Diagram Figure A-70, Timing Diagrams Figures A-59 through A-46).

(1) XMTR 25 ARQ Cycle Control. - The purpose of this block is to check the receiver ARQ flag signal R ARQ FLG at the end of each character transmitted. If the flag is found to be set (HIGH), this block inhibits the data source (No new data requested), then transmits and memorizes two ARQ supervisory characters followed by the contents of the transmitter memory. The number of characters depends upon the memory length selected. At the end of this sequence the receiver ARQ flag signal R ARQ FLG is again checked to see if data has been received correctly; if not, (Flag set HIGH) the transmitter repeats the ARQ sequence.

(a) The block consists of six flip-flops U5A, U5B, U11A, U11B, U18A (Figure A-14), and U10B (Figure A-16); three NAND gates U6B, U6D (Figure A-3), and U1D (Figure A-2); two NOR gates U6A (Figure A-3), and U12C (Figure A-2); and four inverters U17A, U17C, U16D, U3D (Figure A-1).

(b) Flip-flops U5A, U5B, U10B, U11A, U18A are reset and U11B is preset by the initialization signal INIT 2, which clears the ARQ logic sequence. When the receiver raises the ARQ flag, the signal R ARQ FLG is true (HIGH); it is connected to the J input (Pin 8) of flip-flop U10B. At the end of the active character the transmitter timing signal X N L CLK clocks U10B and its Q output (Pin 5) goes HIGH. This is applied to the D input of flip-flop U5A; it also enables the Sync Initiate block (XMTR 26) with the signal ARQ SYNC EN. The

Q output (Pin 6) of U10B goes LOW generating the control signal X ARQ INH, which holds the transmitter step clock and disables the Inhibit Request block (XMTR 23). This signal also generates the memory ARQ marker bit MEM IN 9 via the enabled NAND gate U6B and sets the D input (Pin 12) of flip-flop U11B to be LOW. At this time memory write signals MEM WRITE A and MEM WRITE B write the last data character and the ARQ marker bit MEM IN 9 into the memory, which responds with the signal MEM OUT 9 (LOW). This signal--applied through NOR gate U12C--makes the D input (Pin 12) of flip-flop U11A HIGH. It also enables the NAND gate U6B through NOR gate U6A and inhibits the generation of a sync cycle from the front panel SYNC switch. It is followed by the timing signal X P L CLK. This resets flip-flop U11B; output Q (Pin 9) goes LOW producing the ARQ supervisor inhibit signal ARQ SUP INH. X P L CLK presets flip-flops U18A and U11A. Output Q (Pin 5) of U11A goes HIGH generating the supervisor control signal ARQ GEN through inverter U17A. Output Q (Pin 6) goes LOW disabling NAND gate U1D and generating the ARQ flag clear signal X CL ARQ FLG, which clears the receiver ARQ flag. The Q output (Pin 6) of flip-flop U18A goes LOW holding the D input (Pin 2) on U11A HIGH via the NOR gate U12C.

(c) The transmitter timing signal X PL CLK also increments the memory address counter, which removes the ARQ marker bit, and the signal MEM OUT 9 becomes false (HIGH). This makes the D input (Pin 2) of U18A LOW and removes the second enable on NAND gate U6B via NOR gate U6A. It also enables the front panel SYNC switch as FP SYNC INH becomes false (LOW). At the end of the next character the transmitter timing signal X N L CLK presets flip-flop USA; its Q output (Pin 5) goes HIGH, sets the D input Pin 12) of U5B HIGH, and enables NAND gate U1D (the second input to U1D is disabled by U11A). Its Q output (Pin 6) disables the NAND gate U6B (through U6A). (Pin 4) goes LOW removing ARQ marker bit signal MEM IN 9 The J-K flip-flop U10B has both J and K inputs LOW--because the ARQ flag signal has been reset (LOW), and the memory out signal MEM OUT 9 is false (HIGH). Therefore, its output does not change when clocked. At this time memory write pulse MEM WRITE B writes the generated ARQ supervisory character into memory; this is followed by the next rise of the transmitter clock X CLK 1, which presets flip-flop U5B. Its Q output (Pin 9) goes HIGH, and lights the front panel indicator lamp through driver inverter U3D and resistor R5. The output of inverter U3D also generates the remote ARQ IND signal. The next transmitter timing signal X PL CLK resets flip-flop U13A causing the D input (Pin 2) of flip-flop U11A to be set LOW. The memory address counter is also incremented at this time by the X PL CLK clock signal. At the end of the next character the timing signal X N L CLK has no effect and the next memory write signal MEM WRITE B writes a second ARQ supervisory character into the memory. X PL CLK then resets U11A, which disables the supervisory generator signal ARQ GEN and removes the clear signal X CL ARQ FLG from the receiver ARQ flag. At the same time it enables NAND gate U1D to generate the inhibit signal $\overline{\text{MEM ARQ INH}}$. This

disables memory write signal MEN WRITE B, and the memory parity checker. With the met-nary write signal disabled, the transmitter continues to transmit from the contents of its memory, No new data is accepted from the data source or supervisory characters generated. The memory address counter is incremented after each character has been transmitted: after one complete memory cycle, the ARQ marker bit MEM OUT 9 again becomes true (LOW). The character accepted at the time of the ARQ flag is now on the memory output lines and the receiver may have repeated the ARQ flag. If so, the transmitter repeats the ARQ cycle. The effect of the marker bit MEM OUT 9 on flip-flop U10B is nullified by the raised flag, R ARQ FLG (HIGH); it remains preset. MEM OUT 9 is inverted by U17C and enables NAND gate U6B via NOR gate U6A to generate ARQ marker bit MEM IN 9, which is written into the same location by the MEM WRITE A signal. The transmitter repeats the ARQ sequence, generating two ARQ supervisory characters, clearing the receiver ARQ flag, and repeating the contents of its memory.

(d) If the receiver has not raised the ARQ flag at the end of the last memory character, the timing signal X NL CLK resets flip-flop U10B, which removes the inhibit from the transmitter step clock by making the signal X ARQ INH false (HIGH), and sets the D input (Pin 12) of flip-flop U11B HIGH The ARQ marker bit MEM IN 9 is also set LOW because NAND gate U6B is disabled when the signal X ARQ INH goes false (HIGH). The D input (Pin 2) of flip-flop U5A is set LOW at the same time by the Q output of U10B. At memory write time MEM WRITE B is still disabled and the last character is transmitted from the memory. Also, the ARQ marker signal MEM IN 9 is erased from the memory because MEM WRITE A is never disabled and MEM IN 9 is set false (LOW). The timing signal X PL CLK sets flip-flop U11B; its Q output (Pin 9) goes HIGH forcing the control signal ARQ SUP INIT to be false (HIGH). Now transmitter requests a new character from the data source and converts it into a parallel word. The next X NL CLK clock signal resets flip-flop U5A, disabling NAND gate U1D, and removing the memory write inhibit signal MEM ARQ INH. The D input (Pin 12) of the flip-flop U5B iS also set LOW at this time. The memory write signal MEM WRITE B writes the new character into the memory and the transmitter transmits it. The next rise of the transmitter clock resets flip-flop U5B, which extinguishes the front panel ARQ indicator light and makes the remote ARQ IND signal false (HIGH). The ARQ control logic has now returned to the normal data flow, or initialized state. Timing for the ARQ control sequence is illustrated in figure 4-13. The signals X CL ARQ FLG, MEM ARQ INH and MEM IN 9 can be monitored at the test points TP2, TP3 and TP5 respectively.

(2) XMTR 26 Sync Initiate. - The purpose of this block is to generate the sync cycle start signal ST SYNC CYCLE. The block consists of two flip-flops U8A and U8B (Figure A-16); three NOR gates U1A, U1B (Figure A-2) and U7A (Figure A-6); a NAND gate U7C (Figure A-4), and two inverters U16F (Figure A-1), U2A (Figure A-2). The front panel SYNC initiate switch

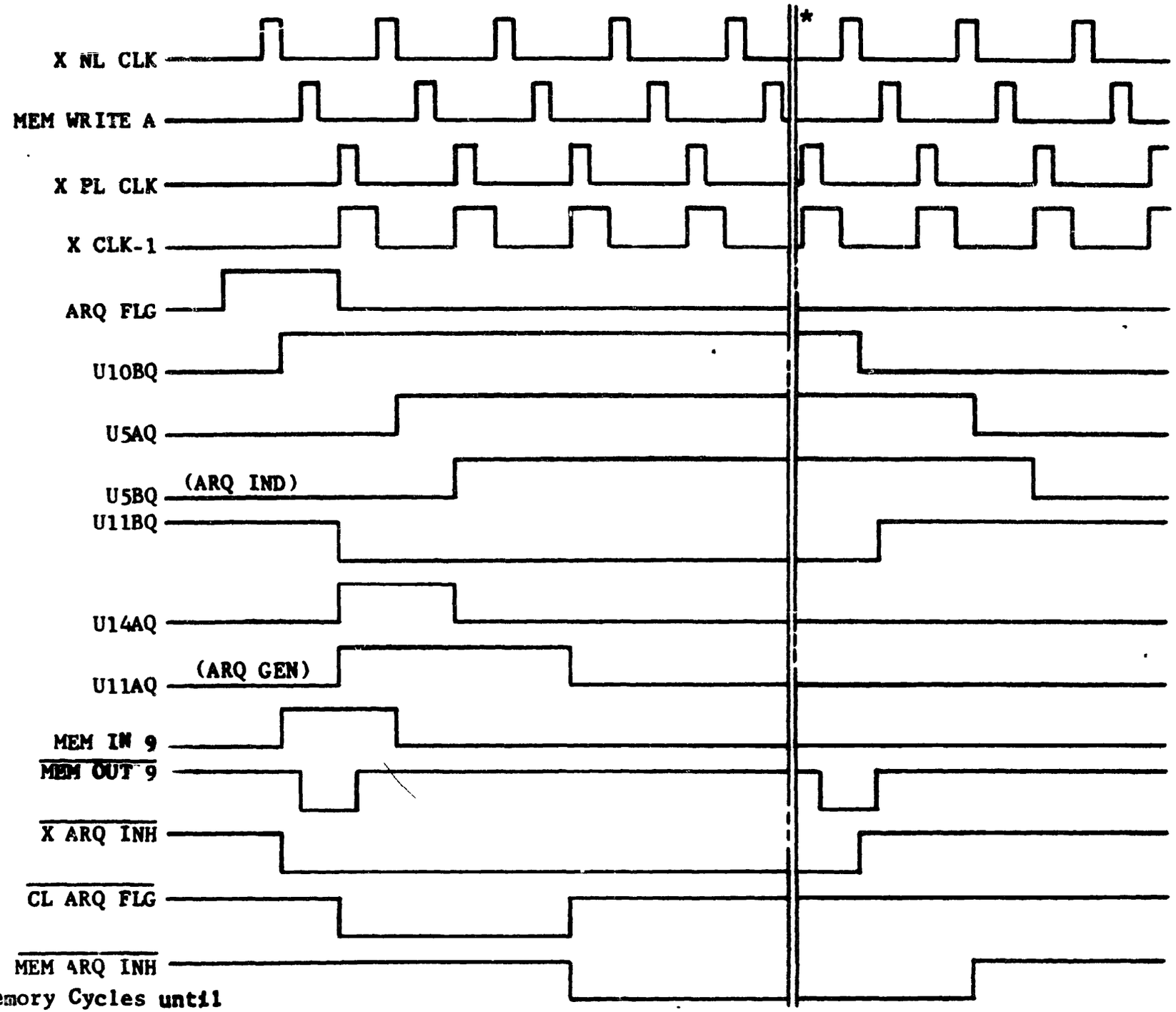


Figure 4-13. XMTR - ARQ Cycle Control Timing Diagram.

generates the signals FP SYNC INT and FP SYNC INT which are de-glitched by the R-S flip-flop consisting of U1A and U7A, then logically OR'ed to the remote sync initiate signal SYNC INIT by negative logic NOR gate U1B. The output (Pin 6) goes HIGH to initiate a sync cycle. This signal is applied to the J input (Pin 1) of flip-flop U3A, and its complement--generated by inverter U16F--is applied to the K input (Pin 4). U8A and U8B are normally reset (both Q outputs LOW), thus disabling NAND gate U7C. When a sync cycle is initiated, the J input (Pin 1) of U8A is HIGH. At the end of the active character timing signal X NE CLK presets U8A; its Q output (Pin 3) goes HIGH, which--if the system is in an ARQ CYCLE (Signal ARQ SYNC EN true (HIGH)-enables NAND gate U7C to generate the sync cycle start signal ST SYNC CYCLE at its output (Pin 8). This signal is inverted by U2A and becomes the J input (Pin 8) of flip-flop U8B, which is preset at the end of the next character by the timing signal X NL CLK and removes ST SYNC CYCLE. The sync cycle start signal is, therefore, active (LOW) for one character time only--after the sync switch or remote line are activated. The timing for sync cycle initiation sequence is shown in Figure 4-14.

(3) XMTR 27 XMTR Sync Cycle Control. - The purpose of this block is to check the receiver sync flag signal SYNC FLG 1 and the local start sync cycle signal ST SYNC CYCLE at the end of each character transmitted and--if active (LOW)--to inhibit the memory output and transmit a resynchronization sequence that is one complete memory cycle long but does not change the contents of the memory. The block consists of three flip-flops U4A, U4B (Figure A-14), U10A (Figure A-16); three NAND gates U9A, U9B (Figure A-7), U1C (Figure A-2); three NOR gates U3B, U2C inverters U3F, U17D (Figure A-1).

(a) Flip-flops U10A and U4B are reset and U4A is preset by initialization signal INIT 2, which clears the sync control logic. The receiver sync flag signal R SYNC FLG 1 and the local start sync cycle signal ST SYNC CYCLE are logically OR'ed by the negative logic NOR gate U3B which when active makes the J input (Pin 1) of flip-flop U10A HIGH. This is clocked at the end of the active character by the timing signal X NL CLK, and it Q output (Pin 2) goes LOW generating the control signal X SYNCING, and enabling NAND gate U9B to generate sync cycle memory marker bit MEM IN 10. Also, NAND gate U1C is disabled, and the D input (Pin 2) of flip-flop U4A is set LOW by the same signal. The Q output of U10A goes HIGH and is directly connected to the D input (Pin 12) of U4B. At this time memory write signal MEM WRITE A writes the sync cycle memory marker bit MEM IN 10 which then generates the signal MEM OUT 10. This adds a second enable to the NAND gate U9B, via inverter U17D and NOR gate U6C. (It should be remembered that the memory write signal MEM WRITE B is disabled because the system is in an ARQ cycle). Three microseconds later X L PS CLK presets the flip-flop U4B. Its Q output (Pin 9) generates the start sync sequence signal ST SYNC SEQ and enables input (Pin 9) of NAND gate U1C but input (Pin 10)

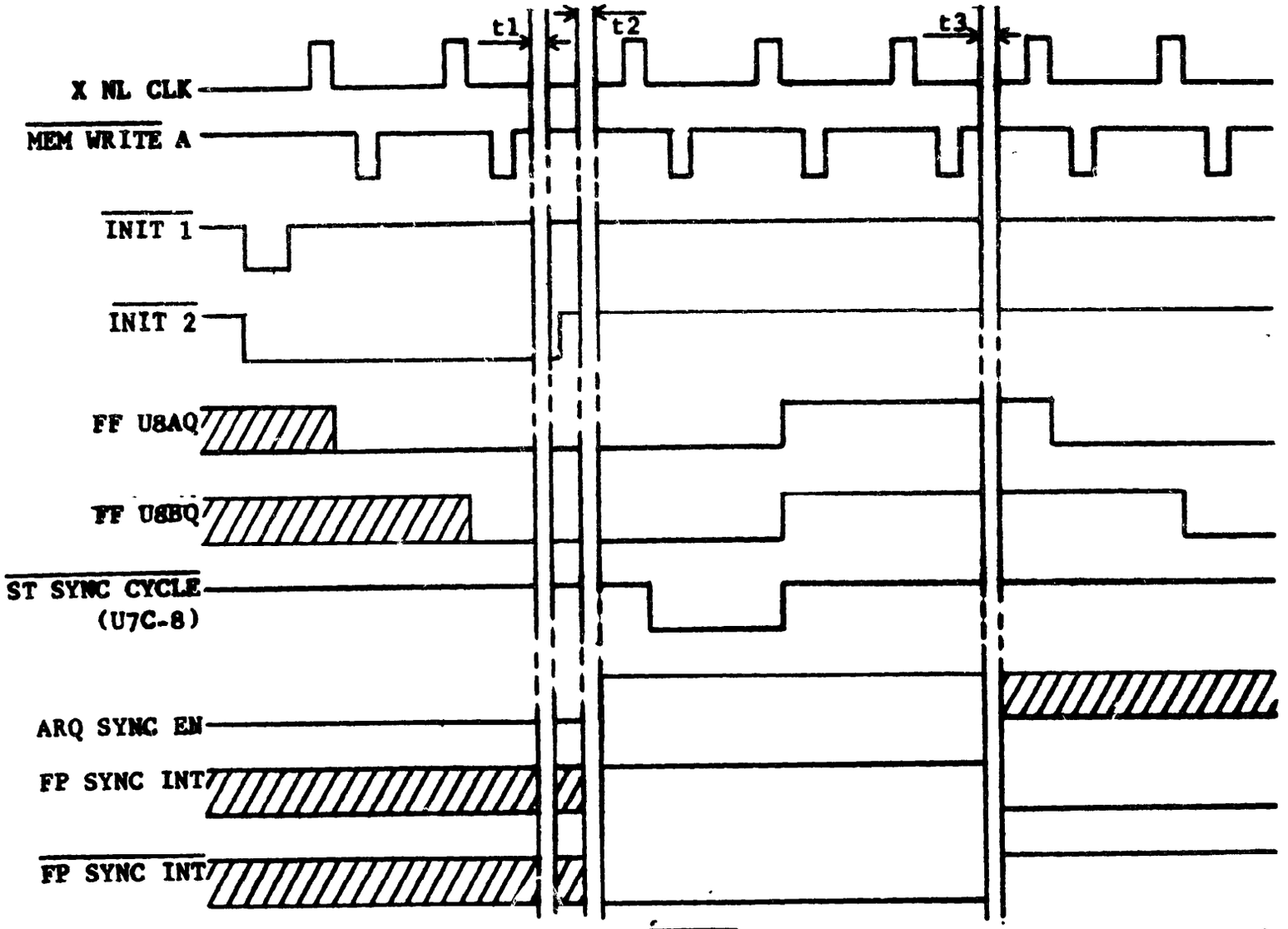


Figure 4-14. Sync Cycle Initiate Timing Diagram.

is disabled by the signal X SYNCING, which prevents the receiver flags being cleared at this time. The Q output removes the first enable from U9B via NOR gate U6C. The rise of the transmitter clock signal X CLK 1 resets U4A its Q output goes LOW and-through NOR gate U2C and driver inverter U3F--lights the front panel indicator SYNC, and generates the remote signal SYNC IND.

(b) The next timing signal X PL CLK increments the memory address counter, removing the sync cycle marker bit MEM OUT 10. It also disables the memory output data via transmitter block (XMTR 29) and generates the SYNC A supervisory character via the transmitter blocks (XMTR 28) and (XMTR 32). This is transmitted as the next character followed by the SYNC B character and a series of Inhibit Activate or Inhibit Deactivate supervisory characters, depending upon the position of the inhibit switch on the front panel. When the transmitter is transmitting the Inhibit Activate or Inhibit Deactivate supervisory signals, the control signal lNH A/D EN is true (LOW) and enables an input (Pin 4) of NAND gate U9A. When the receiver correctly receives either the Inhibit Activate or the Inhibit Deactivate supervisory characters, it must be correctly synchronized. To signify this, it sends the sync flag signal R SYNC FLG 2, which enables another input (Pin 5) of NAND gate U9A. The transmitter memory address counter is incremented after each character, and after one complete memory cycle the sync cycle memory marker bit MEM OUT 10 goes true (LOW). This enables another input (Pin 2) of U9A. lf all the receiver flags are received, its output goes HIGH and inputs J and K of U10A are HIGH. Therefore, the next timing signal X NL CLK toggles the flip-flop and the signal X SYNClNG goes false (HIGH). This sets the D input (Pin 2) of flip-flop U4A HIGH, and enables NAND gate U1C to generate the signal X CL SYNC FLGS, clearing both receiver sync flags. NAND gate U9B is also disabled at this time, removing sync cycle memory marker bit MEM IN 10, and the D input (Pin 12) of flip-flop U4B goes LOW.

(c) The next memory write signal MEM VVRITE A erases the sync cycle marker bit; timing signal X L PS CLK transmits the last inhibit supervisory character and resets flip-flop U4B, which removes the start sync sequence signal ST SYNC SEQ, and disables NAND gate U1C, removing the clear signal X CL SYNC FLGS. It also enables the NAND gate U9B via NOR gate U6C. The rise of the transmitter clock signal X CLK 1 presets flip-flop U4A and its Q output (Pin 6) goes HIGH, removing the transmitter enable for the sync cycle indicator. The next X PL CLK signal removes the inhibit from the memory output and the transmitter resumes the ARQ sequence. If either of the receiver flags R SYNC FLG 1 or R SYNC FLG 2 have not been received, flip-flop U10A is not toggled. The sync cycle memory marker bit MEM OUT 10 enables NAND gate U9B through inverter U17D and NOR gate U6C, generating the sync marker bit MEM IN 10. This causes the transmitter to repeat the SYNC CYCLE until the local receiver is synchronized

with the distant transmitter (which also implies that the distant receiver is synchronized to the local transmitter). Test points are provided to monitor the signals X CL SYNC FLGS (TP1) and MEM IN 10 (TP4). The timing is illustrated in Figure 4-15.

(4) XMTR 28 Sync Cycle Supervisor Control. - This block controls the sequence of generating the supervisory signals SYNC A GEN, SYNC B GEN, and INH A/D EN, in the correct order. The block consists of two flip-flops U14A and U14B (Figure A-16); six NAND gates U15A, U15B, U15C, U2D, U13A (Figure A-2); two NOR gates U13C (Figure A-2, and U7B (Figure A-4), and three inverters U16A, U16B, U16C (Figure A-1). The two flip-flops U14A and U14B are both reset by the initialization signal INIT 2. They are connected as a 2-bit counter, clocked by the timing signal X PC CLK.

(a) The sync cycle sequence is started when the control signal ST SYNC SEQ goes true (HIGH) and sets the J-input (Pin 1) of flip-flop U14A HIGH. The next timing signal, X PL CLM, sets the flip-flop causing its Q output (Pin 3) to go HIGH: this enables NAND gate U15D, which generates the supervisory control signal SYNC A GEN. SYNC A GEN enables NAND gate U15C through inverter U16B; its output, inverted in U16C, set the J input (Pin 8) of U14B HIGH. NAND gate U2D is also enabled (sync cycle memory marker bit MEM OUT 10 is false (HIGH) and its output sets the K input (Pin 4) of flip-flop U14A HIGH (through NOR gate U13C). The transmitter now transmits the supervisory character SYNC A; the next timing signal X PL CLK presets flip-flop U14B and toggles (resets) flip-flop U14A (both inputs J and K set HIGH). This disables NAND gate U15D, removing the signal SYNC A GEN and enabling NAND gate U15B to generate the supervisory control signal SYNC B GEN. The two NAND gates U2D and U15C are also disabled. As a result, the J input (Pin 8) of flip-flop U14B and the K input (Pin 4) of flip-flop U14A both go LOW. The transmitter sends the supervisory character SYNC B and the next timing signal X PL CLK presets flip-flop U14A. (Both J and K inputs of flip-flop U14B are LOW, so it does not change state). This disables NAND gate U15B, removing the signal SYNC B GEN, and enabling NAND gate U15A, which generates control signal INH A/D EN and--through inverter U16A--supervisory control signal INH A/D EN.

(b) The transmitter now sends the supervisory character Inhibit Activate or Inhibit Deactivate but the next timing signal X PL CLK has no effect on the sync cycle supervisor control block. The flip-flops remain unchanged. Hence the transmitter continues to transmit the Inhibit Activate or Inhibit Deactivate supervisory character, incrementing the memory address counter, but not changing the memory contents after each character transmitted. When the sync cycle memory marker bit MEM OUT 10 becomes true (LOW) after one complete memory cycle, XMTR 27 (Sync Cycle Control) removes start sync sequence signal ST SYNC SEQ--if the receiver has sent both sync flags, R SYNC FLG 1 and R SYNC FLG 2. Removal of ST SYNC

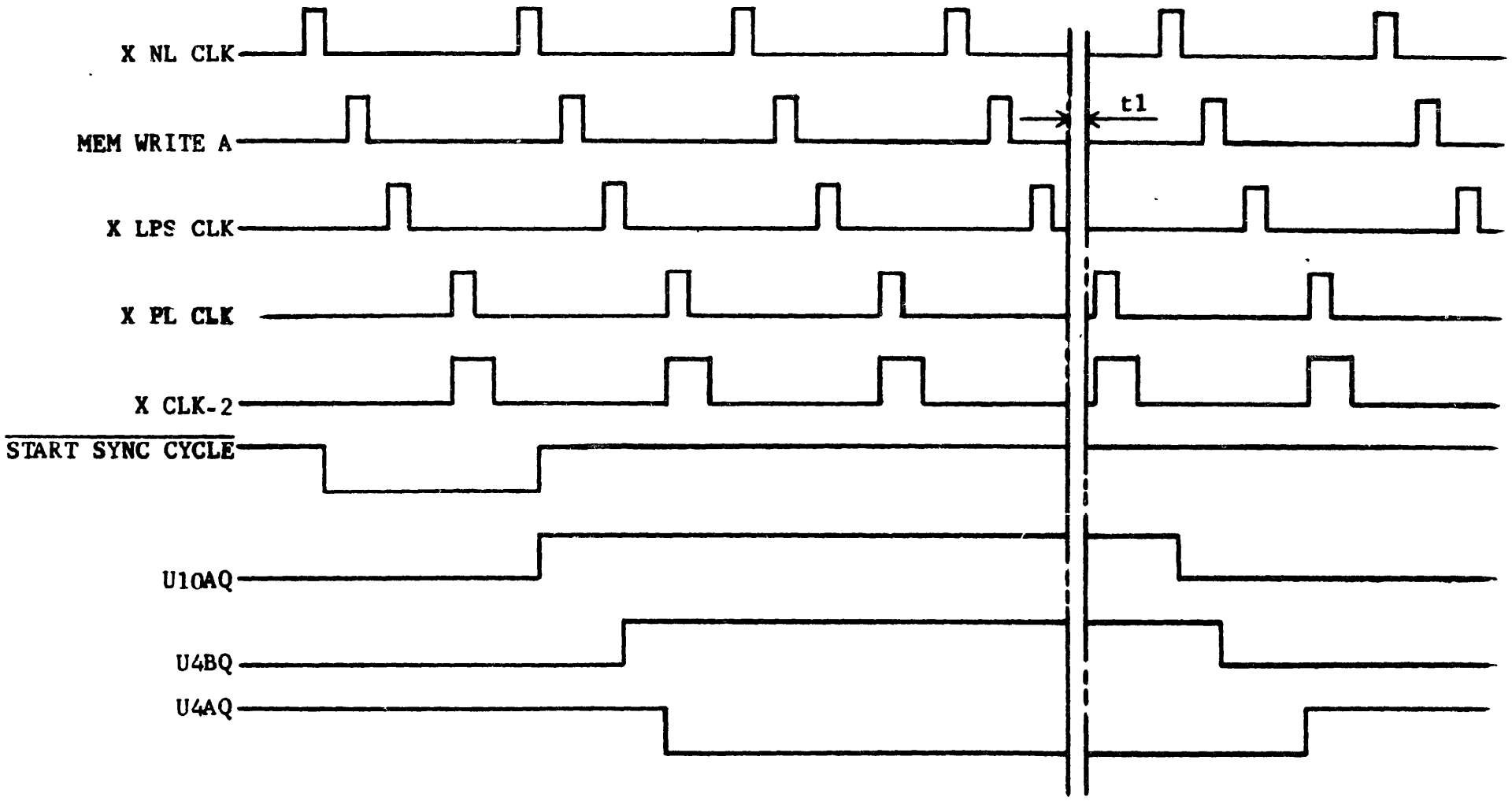
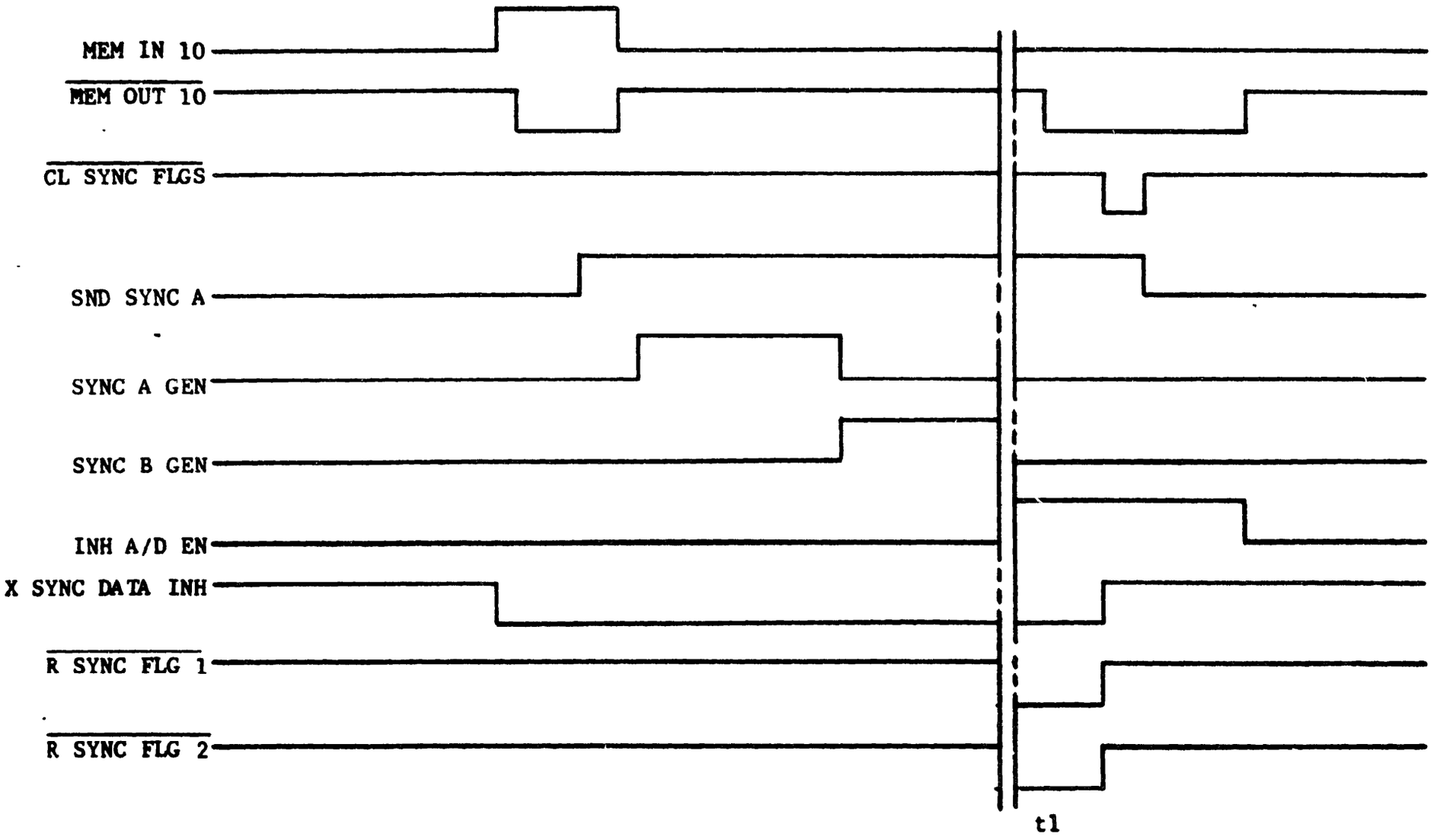


Figure 4-15. XMTR Sync Control Timing Diagram and Sync Cycle Supervisor Control Timing Diagram Sheet 1 of 2.



t1 - indeterminate time until R SYNC FLG 1 and R SYNC FLG 2 are both low

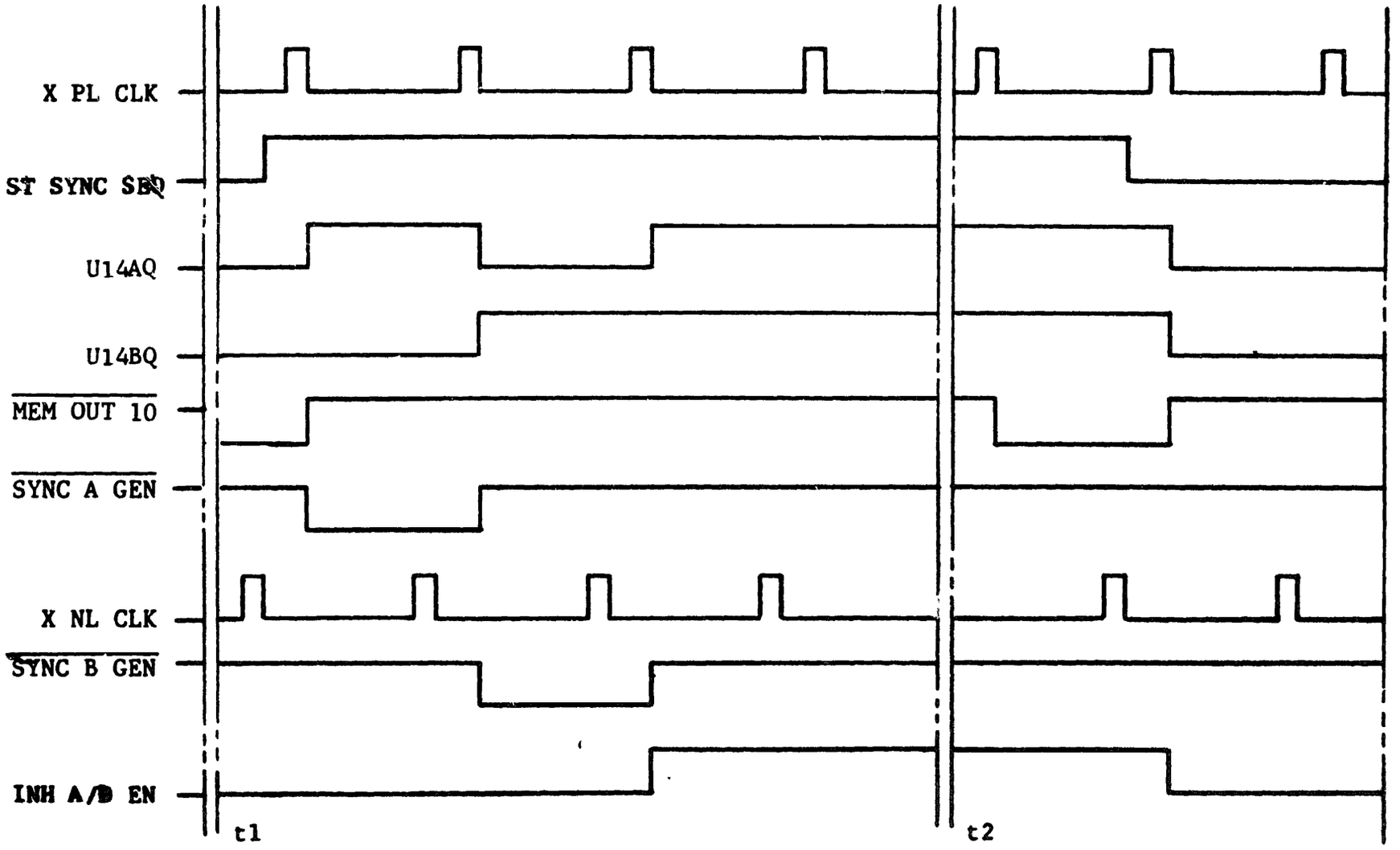
Figure 4-15. XMTR Sync Control Timing Diagram and Sync Cycle Supervisor Control Timing Diagram Sheet 2 of 2.

SEQ makes the K inputs of both flip-flops U14A and U14B HIGH through negative logic NOR gates U13C and U7B. The next timing signal X PL CLK resets flip-flops U14A and U14B returning the counter to the initial condition. If the receiver has not resynchronized, the XMTR Sync Cycle Control block (XMTR 27) repeats the sync cycle; but the MEM OUT 10 signal enables NAND gate U13A, setting the K input (Pin 11) of flip-flop U14B HIGH via the negative logic NOR gate U7B. The timing signal X PL CLK resets flip-flop U14B and supervisory control signal SYNC A GEN becomes active, thus repeating the sync sequence. Output signals SYNC B GEN, INH A/D EN, and SYNC A GEN, can be monitored at test points TP6, TP7, and TP8 respectively. The timing is illustrated in Figure 4-16.

f. A2A5 Constant Ratio Code Generator (Logic Diagram Figure A-44, Block Diagram Figure A -33, Wiring Diagram Figure A-71, and Timing Diagrams Figures A-59 and A-64).

(1) XMTR 29 Sync Cycle Data Inhibit. - The purpose of this block is to inhibit the memory output data lines during a transmitter resynchronization sequence, It does this by forcing them all into a HIGH state. The block consists of a control flip-flop U7B (Figure A-14); and nine NAND gates U12A, U12B, U12C, U12D, U13A, U13B, U13D, U14A, U14B (Figure A-2). The sync cycle control signal X SYNCING is connected to the D input (Pin 12) of control flip-flop U7B; when true (LOW), it disables all the NAND gates after timing signal X PL CLK clocks the flip-flop. Hence, during a sync cycle, the outputs of all the NAND gates in this block are HIGH and independent of the memory output data signals.

(2) XMTR 30 Sync Cycle Activate or Deactivate Generator. - This block generates the Inhibit Activate or Inhibit Deactivate supervisory character that is not stored in memory, but is required by the resynchronizing sequence. It consists of two NAND gates U6C and U6D (Figure A-2); seven NOR gates U20A ,U20B,U20C, U20D, (Figure A-2), U21A, U218, U21C (Figure A-4); and four inverters U5B (Figure A-4) U16A, U22A, U22B (Figure A-l). The control signal SYNC INH A/D is determined by the front panel INHIBIT ACTIVATE/DEACTIVATE switch or remote control signal LOCAL INH, and is LOW to generate the Inhibit Deactivate and HIGH to generate the Inhibit Activate supervisory character. NAND gates U6C and U6D are enabled by the supervisor generator signal INH A/D EN. The state of control signal SWITCH INH A/D determines whether U6D or U6C is active, LOW. If SWITCH INH A/D is HIGH, the output of U6C goes LOW generating the Inhibit Activate supervisory character: but if SWITCH INH A/D is LOW, the output of U6D goes LOW generating the Inhibit Deactivate supervisory character. The supervisor marker signal SUPER BIT goes active HIGH when either supervisor character is transmitted it can be monitored at the test point TP7.



t1 - indeterminate time until $\overline{\text{SND SYNC A}}$ goes high

t2 - indeterminate time until $\overline{\text{MEM OUT 10}}$ goes low
(complete Memory recirculation)

Figure 4-16. Sync Cycle Supervisor Control Timing Diagram.

(3) XMTR 31 Constant Ratio Code Encoder. - The purpose of this block is to encode the incoming terminal codes into Constant Ratio Codes in which every combination has four 1's, and either four or seven 0's, depending upon the selected format. The block consists of three 1024-Bit Read-Only Memories U17 (Figure A-24D), U18 (Figure A-24E), and U19 (Figure A-24C), each arranged with 256 addresses and four output bits per address. The outputs of the three ROM's generate the constant ratio code. The twelfth output is unused in all formats: pull-up resistors R2 through R13 are required because the ROM's have open collector outputs. The 256 addresses for each ROM are connected in parallel, and each address represents one of the input terminal codes (in 8-Bit Start-Stop there are 256 different input codes). Therefore, the programming of the three ROM's generates a constant ratio code for each of the input terminal codes supplied to it as different address. The logic is static--no clock is required; but some time is required for the constant ratio codes to be generated.

(4) XMTR 32 Sync Cycle SYNC A and SYNC B Generator. - The purpose of this block is to generate the resynchronization sequence SYNC A followed by SYNC B, which generates eight sequential P's followed by four or seven O's depending upon format selected. The block consists of five NAND gates U1A, U15A, U15B, U15D, (Figure A-2) U9A (Figure A-6); fifteen NOR gates U1B, U1C, U1D, U8A, U8B, U8C, U8D, U10A, U10B, U10C,- U10D, U11A, U11B, U11D (Figure A-2), U9B (Figure A6E and five inverters U16B, U16D, U16E, U16F (Figure A-1) U15C (Figure A-2).

(a) The supervisory character SYNC A is the same in all formats selected; it is generated--after the constant ratio code encoder--by the supervisory control signal SYNC A GEN. This forces the shift register U3 (Figure A -20) in XMTR 33 to be loaded with all l's, via the NOR gates U10A, U10B, U10C and U10D. It also resets to O's shift register U2 and U4 (Figure A-20) in XMTR 33 via the gates U15C, U15D, U8C and U15B. Thus the SYNC A supervisory character is loaded into the shift register during last bit time by the timing signals X PS CLK and X BIT LAST.

(b) The supervisory character SYNC B depends upon the format selected, It is controlled by the format signal CODE 8 -BIT, and its complement CODE 11-BIT. They enable the NAND gates U1A or U9A. In 8-bit constant ratio codes NAND gate U1A is enabled and its output (Pin 3) goes LOW; this forces the shift register U2 on XMTR 33 to be loaded with all l's via NOR gates U1B, U1D, U1C, and U9B. The inverted control signal SYNC B GEN resets shift register U3 on XMTR 33 to all 0's at last bit time via the NAND gate U15A. The shift register U4 on XMTR 33 is not used for 8-bit constant ratio codes, hence the correct supervisory character SYNC B is generated. In 11-bit constant ratio code NAND gate U9A is enabled and its output (Pin 6) goes LOW. This forces the first three bits of shift register U2 in XMTR 33 to be loaded with all 0's via the NOR gates U8B, U1B, U8A,

U1D, U8D, U1C. Also, the last bit of U2 and the three used bits of shift register U4 in XMTR 33 are loaded with all 1's via the NOR gates U9B, U11A, U11B, and U11D, thus generating the correct SYNC B supervisory character in the 11-bit constant ratio code. The supervisory marker signal SUPER BIT is true (LOW) when any of the supervisory characters IDLE, ARQ, INHIBIT ACTIVATE or INHIBIT DEACTIVATE are to be transmitted. Its function is to distort the constant ratio code generated by the ROM (XMTR 31) into the correct constant ratio code for the supervisory character--which cannot be generated directly by the ROM (only 256 addresses available). The supervisor marker signal SUPER BIT resets shift register U4 in XMTR 33 to all O's (one bit of this register is normally set HIGH by the ROM's) and sets the last bit of shift register U2 in XMTR 33 HIGH via NOR gate U9B. (This bit is normally set LOW by the ROM's.)

(5) XMTR 33 Parallel-To-Serial Converter. - The purpose of this block is to convert the 8- or 11- bit constant ratio code into a serial sequence of output data bits timed so that the output data changes at the rise of the transmitter clock. The block consists of an 11- bit shift register composed of U3, U2, and U4 (Figure A-2); two NAND gates U5C (Figure A-4), U11C (Figure A-2); a NOR gate U6A (Figure A-2); an inverter U22C (Figure A-1); and a flip-flop U7A (Figure A-14). The 11-bit shift register U3, U2 and U4 is parallel loaded during transmitter last bit time by the timing signal X PS CLK (which, during last bit time occurs 3 microseconds after the memory write pulse--giving the static logic plenty of time to settle). The register is then shifted from left to right by the timing signal X PS CLK which occurs once per bit time (l's are loaded into U3 as the data is shifted out). The constant ratio code length is selected by NAND gates U5C and U11C, which are enabled by the format signals CODE 8 BIT and CODE 11 BIT so that the output QC (Pin 13) on shift register U4 is selected as the output in the 11-bit constant ratio code, This can be monitored at test point TP6. The output QD (Pin 12) on shift register U2 is selected as the output in the 8-bit constant ratio code (Monitored at test TP5). The two different formats are logically OR'ed by NOR gate U6A and retimed to the rise of the transmitter clock X CLK 1 by flip-flop U7A, which is held preset during the first part of system initialization by the signal INIT 3. The output signal SEND LIN can be monitored at test TP3. It is inverted by the line driver into the signal SEND LIN L. Inverter U22C generates timing signal X BIT LAST for the SYNC A and SYNC B Generator XMTR 32 from the X BIT LAST input. Timing for the parallel-to-serial converter is illustrated in Figures A-60 through A-64.

(6) XMTR 34 Format Switch Decoder. - The purpose of this block is to generate the binary load signals for the Sample Enable Counter (XMTR 10) and the format control signals used to determine the length of the constant ratio code transmitted. The block consists of five NOR gates U6B, U13C, U14C, U14D (Figure A-2) U5A (Figure A-4); and four inverters U16C, U22D U23E, U22F (Figure A-1). The control signals BIT STREAM, 5 BIT S-S

6 BIT S-S, 7 BIT S-S, 7 BIT S-S and 8 BIT S-S from the format switch are coded into the output signals SMPL CTR 1, SMPL CTR 2, SMPL CTR 4, and SMPL CTR 8 in accordance with the truth table, Table 4-9. In addition, the control signal BIT STREAM is generated from BIT STREAM by inverter U16C; and the format control signal CODE 8 BIT is generated by NOR gate U6B if either BIT STREAM or 5 BIT S-S is true (LOW). The format control signal CODE 11 BIT is generated from CODE 8 BIT by inverter U22E. The binary load signals for the sample enable counter can be monitored at the test points TP1, TP2, TP4 and TP8. (The pull-up resistors for the format switch R16, R11, R10, R9, and R8 are located on circuit board assembly A2A2.)

g. A2A6 Data Input Code and Memory Counter (Logic Diagram Figure A-25, Block Diagram Figure A-34 Wiring Diagram Figure A-72 and Timing Diagrams Figures A-59 and A-64).

(1) XMTR 35 Serial-To-Parallel Converter. - This block converts the incoming serial data into parallel codes, each eight bits wide. The block consists of an 8-bit shift register U8 (Figure A-21). The incoming serial data is connected to the serial input A and B (Pins 1 and 2) and is clocked by the timing signal X SP CLK, which occurs once per bit time at the center of each bit (The incoming data can have any phase relationship with respect to the transmitter clock X CLK 1). Shift register U8 is never reset to all O's ; hence all new data has to be shifted in by timing signal X SP CLK. The incoming data signal X IN DA DL can be monitored at test point TP2. Timing is illustrated in the timing diagrams, Figures A-60, 61 thru 64.

(2) XMTR 36 Memorized Supervisor Data Inhibit. - The purpose of this block is to inhibit the output of the serial-to-parallel converter when a memorized supervisor is to be transmitted (all supervisors except those transmitted during a resynchronization cycle) and to set up the last two bits of the parallel data word when bit stream, 5-bit S-S, or 6-bit S-S formats are selected. The block consists of nine NAND gates U1A, U1B, U15A, U15B, U15C U15D, U10D, (Figure A-2) U11A, U13B (Figure A-4) a NOR gate U10A (Figure A-2) and two inverters U19A (Figure A-1) and U10C (Figure A-2). The inhibit signal X DA/SUP inhibits all the NAND gates (all data outputs HIGH) when active (LOW), and allows normal data flow when inactive (HIGH). The format signals BIT STREAM and 5 BIT S-S are logically OR'ed in NOR gate U10A and the inverted signal sets the last two data bits always to O's (LOW). In 6-bit start-stop format the format signal 6 BIT S-S sets the last data bit always to 1 (HIGH) via inverter U19A and NAND gate U10D.

(3) XMTR 37 Memorized Supervisor Generator. - The purpose of this block is to generate the supervisory characters IDLE, ARQ, INHIBIT ACTIVATE and INHIBIT DEACTIVATE. The block consists of six NOR gates U17D (Figure A-2) U16A, U16B, U9A, U9B (Figure A-6) and U2 (Figure A-8) and two inverters U3A, U3B (Figure A-1). The outputs of these eight gates form the

parallel data code that is stored in the transmitter memory. When a supervisory character is to be transmitted, the output of the serial-to-parallel converter is inhibited, signals are active (LOW)--IDLE GEN, ARQ GEN, ACT GEN or DEACT GEN. The Memorized Supervisor Control block (XMTR 38) sets the ninth memory bit (supervisor marker) MEM IN 8 HIGH to change the constant ratio code into the required supervisor. The codes generated are illustrated in Table 4-10, which shows the actual code stored in the memory, the constant ratio code generated by the read only memory, and the way this is distorted by the supervisor marker signal SUPER BIT in the parallel-to-serial converter (XMTR 33), on circuit board A2A5, to generate the required constant ratio code for each supervisor, (The first three bits, X CODE 0, X CODE 1, and X CODE 2, are all set to 0 (LOW) and X CODE 3 is set to 1 (HIGH).

(4) XMTR 38 Memorized Supervisor Control. - This block controls the data inhibit and the generation of all memorized supervisory characters. It also inhibits the memory write signal during an ARQ cycle. The block consists of a control flip-flop U12A (Figure A-14); seven NAND gates U4, U4C, U5D, U17C (Figure A-2); U11B, U11C (Figure A-4), U18 (Figure A-8); two NOR gates U4A, U4D (Figure A-2); and seven inverters U3C, U3D, U3F, U19B, U19C, U19D, U19E (Figure A-1).

(a) The sample enable signal X DA SMPL EN is true (LOW) after the start bit has been detected in start-stop modes and at first bit time after the transmitter step clock signal in bit stream mode. It is connected to the D input (Pin 2) of flip-flop U12A. This flip-flop is preset by the initialization signal INIT 2 and is clocked at the beginning of the third transmitter bit time by the timing signal X BIT 3. If the start bit has not been detected at this time (X DA SMPL EN false-- HIGH). The B output (Pin 6) goes LOW, producing the control signal X DA/SUP. This signal disables the normal data flow through the Memorized Supervisor Data Inhibit XMTR 36. The Q output (Pin 5) of flip-flop U12A goes HIGH, which enables the NAND gates U5D and U18. NAND gate U5D generates the supervisor marker bit MEM lN 8 for the memory (Test Point TP3). NAND gate gate U18--with normal data flow all inputs are HIGH except Pin 6--generates the supervisory control signal IDLE GEN, which causes the idle supervisory character to be transmitted. Thus, if the data source does not respond to the transmitter step clock within two bit times in any start-stop mode, the transmitter sends an Idle supervisory character.

(b) When an ARQ supervisor is transmitted, the XMTR ARQ control block (XMTR 25) on circuit card A2A4 inhibits the transmitter step clock, holding the data sample signal X DA SMPL EN false (HIGH), which inhibits the data flow and generates the supervisor marker bit MEM lN 8. The XMTR ARQ control block also generates the signal ARQ SUP lNH, which inhibits the generation of Idle, Inhibit Activate, or Inhibit Deactivate. NAND

Table 4-10. Memorized Supervisory Characters

SUPERVISOR CHARACTER	MEMORY INPUT MEM IN 0 MEM IN 1 MEM IN 2 MEM IN 3 MEM IN 4 MEM IN 5 MEM IN 6 MEM IN 7 MEM IN 8	CONSTANT RATIO CODE FROM ROM'S X CODE 0 X CODE 1 X CODE 2 X CODE 3 X CODE 4 X CODE 5 X CODE 6 X CODE 7 X CODE 8 X CODE 9 X CODE 10
$\overline{\text{IDLE GEN}}$	0 1 0 0 0 0 1 1 1	0 1 0 0 0 1 0 0 1 1 0
$\overline{\text{ARQ GEN}}$	0 1 1 0 0 0 0 1 1	1 0 0 0 1 1 0 0 0 1 0
$\overline{\text{ACT GEN}}$	1 1 1 0 0 0 0 1 1	1 0 0 0 1 1 0 0 1 0 0
$\overline{\text{DEACT GEN}}$	1 0 1 1 0 0 1 0 1	1 0 0 0 1 1 0 1 0 0 0

SUPERVISOR CHARACTER	CONSTANT RATIO CODE TRANSMITTED X CODE 0 X CODE 1 X CODE 2 X CODE 3 X CODE 4 X CODE 5 X CODE 6 X CODE 7 X CODE 8 X CODE 9 X CODE 10
$\overline{\text{IDLE GEN}}$	0 0 0 1 0 1 0 0 1 1 0
$\overline{\text{ARQ GEN}}$	0 0 0 1 1 1 0 0 0 1 0
$\overline{\text{ACT GEN}}$	0 0 0 1 1 1 0 0 1 0 0
$\overline{\text{DEACT GEN}}$	0 0 0 1 1 1 0 1 0 0 0

gates U18, U4C, U11B, U4B, and U11C perform this function along with ARQ GEN, which generates the ARQ supervisory character via the Memor - ized Supervisor Generator block (XMTR 37). The supervisory control signal ARQ GEN can be monitored at test point TP6.

(c) When an Inhibit Activate supervisor is transmitted, the Inhibit Request Control block (XMTR 23) on circuit card assembly A2A3 halts the step clock for one character, holding the control signal X DA SMPL EN false (HIGH), which inhibits the data flow and generates the supervisory marker bit MEM IN 8. The Inhibit Request Control block also generates--for one character time--the signal INH ACT GEN (test point TP5), which inhibits (in U18) the generation of the Idle supervisory character. The signal ACT GEN is produced by gates U19C, U4C, U4D and U3F. ACT GEN generates the Inhibit Activate supervisory character via the Memorized Supervisor Generator (XMTR 37).

(d) The logic for the generation of the Inhibit Deactivate supervisory character is identical to the Inhibit Activate and is controlled by the signal INH DEACT GEN (test point 7). The control signal INH SWITCH A/D is HIGH when the front panel inhibit switch or remote line is set for Inhibit Activate; it enables the (Pin 3) input of NAND gate U11B. INH SWITCH A/D is LOW when the front panel inhibit switch or remote line is set for Inhibit Deactivate, which enables the (Pin 11) input of NAND gate U11C through inver- ter U19D. NAND gates U11B and U11C are enabled by the control signal INH GEN through inverter U19E; this signal also inhibits the generation of the Idle supervisory character via NAND gate U18. The control signal INH GEN is generated by the Inhibit Received Control block (XMTR 22) on Circuit board assembly A2A3 when an Inhibit Activate supervisory character is re- ceived (with the strap option in the "A" position). This causes the trans- mitter to transmit constantly either the Inhibit Deactivate or Inhibit Activate supervisory character (dependent upon control signal SWITCH INH A/D).

(e) The supervisory marker bit MEM IN 8 and the memory B write signal MEM WRITE B are inhibited by the control signal MEM ARQ INH, which is true (LOW) after the second character of an ARQ cycle. It prevents the B memory from being changed during the ARQ cycle.

(5) XMTR 39 Memory Address Counter. - This block identifies each memory location with an address and determines the length of the memory being used. The blockconsists of a 4 bit Counter U14 (Figure A-19), three flip-flops U6A, U6B (Figure A-16) U12B (Figure A-14); eight NAND gates U1C, U5A, U17B, U21A, U21B, U21C, U21D (Figure A-2) U13A (Figure A -4); sixteen inverters U1D, U5C, U7A, U71B, U7C, U7D, U17A, U17B, (Figure A -2); U3E, U19B, U20A, U20B, U20C, U20D, U20E, U20F (Figure A-1); and a NOR gate U5B (Figure A-2).

(a) The counter is initialized by the initialization signal $\overline{\text{INIT 1}}$, which resets flip-flops U6A, U6B, and U12B, and loads counter U14 with the complements of memory length control signals MEM LG 4, MEM LG 8, MEM LG 16 and MEM LG 32, via the NOR gate U5B and inverter U3E. The counter is loaded directly when the load (Pin 11) goes LOW--no clock is required. The truth table for the memory length control signals is given in Table 4-11. Flip -flops U6A and U6B form a 2-bit, bit synchronous counter that is always enabled and counts the number of transmitted characters being clocked by the timing signal X PL CLK. The outputs of this counter generate the first two memory address signals MEM ADD 1 and MEM ADD 2 via the inverter drivers U7D and U7C. The 2-bit counter (U6A and U6B) must be at maximum count (four) to make the memory address lines both 0. It is incremented once per character by the timing signal X PL CLK. After two characters, NAND gate U13A is enabled so that the next X PL CLK also clocks flip-flop U12B via the gates U13A, U5C and U19B. U12B tests counter U14 for maximum count--indicated by Pin 12 going HIGH. This output is connected to the D input (Pin 12) of flip-flop U12B via gates U17A and U17B; it presets U12B when counter U14 is at maximum count. When preset, U12B generates the control signal MEM ADD MAX for four character times. This enables NAND gate U1C to load counter U14 with the complement of the memory len length control signals MEM LG 4, MEM LG 8, MEM LG 16 and MEM LG 32 at the rise of the next timing signal X PL CLK, which occurs slightly after the fall of the signal X PL CLK. The complement signal MEM ADD MAX is used during the initialization sequence to remove the signal INIT 3 after one complete memory length has been initialized. It also disables NAND gate U5A preventing counter U14 being clocked at the maximum count of the 2-bit counter (U6A and U6B). After three characters have been counted by U6A, U6B NAND gate U17B is enabled and its output (Pin 6) goes LOW, enabling counter U14 to be incremented by the next timing signal X PL CLK via NAND gate U5A. Hence counter U14 is incremented once every four characters until maximum count (fifteen) is reached; then it is loaded with the complement of the memory length control signals, to the starting count, and the sequence repeats. The output of counter U14, QA (Pin 3), QB (Pin 2), QC (Pin 6), and QD (Pin 7), generate the four most significant memory address signals, MEM ADD 4, MEM ADD 8, MEM ADD 16, and MEM ADD 32 via inverter drivers U7B, U7A, U20B, and U20C. When counter U14 is at maximum count (fifteen), the memory address signals are all LOW. The timing is illustrated in Figure 4-17.

(b) If the memory length switch is set at position 1 for a memory length of eight characters, the counter U14 is loaded with a count of 14; it is incremented to 15 (maximum count) after counting four characters and reloads back to 14 after counting four more characters, thus generating a sequence of eight counts that produce the binary address of each memory location. In this example only the first three memory address signals change state. When the memory length switch is set to position 15, for a memory

Table 4-11. Memory Length Control Signals

SWITCH POSITION	MEMORY LENGTH	MEMORY LENGTH CONTROL SIGNALS			
		MEM LG 4	MEM LG 8	MEM LG 16	MEM LG 32
0	4	LOW	LOW	LOW	LOW
1	8	HIGH	LOW	LOW	LOW
2	12	LOW	HIGH	LOW	LOW
3	16	HIGH	HIGH	LOW	LOW
4	20	LOW	LOW	HIGH	LOW
5	24	HIGH	LOW	HIGH	LOW
6	28	LOW	HIGH	HIGH	LOW
7	32	HIGH	HIGH	HIGH	LOW
8	36	LOW	LOW	LOW	HIGH
9	40	HIGH	LOW	LOW	HIGH
10	44	LOW	HIGH	LOW	HIGH
11	48	HIGH	HIGH	LOW	HIGH
12	52	LOW	LOW	HIGH	HIGH
13	56	HIGH	LOW	HIGH	HIGH
14	60	LOW	HIGH	HIGH	HIGH
15	64	HIGH	HIGH	HIGH	HIGH

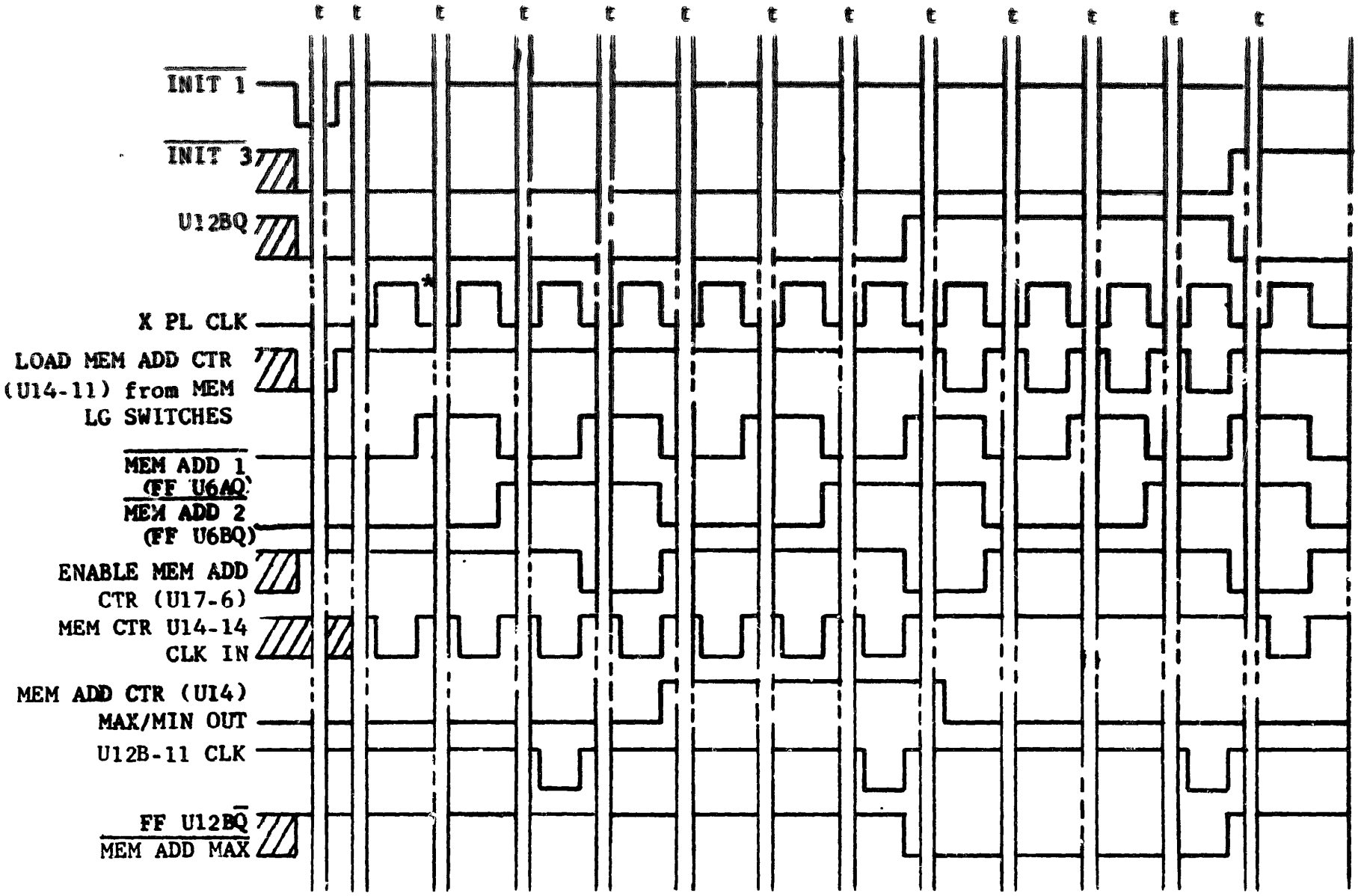


Figure 4-17. Memory Address Counter Timing Diagram

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length of 64 characters, all six memory address signals change state. The two most significant memory address signals MEM ADD 16 and MEM ADD 32 are coded into the four chip select signals $\overline{\text{MEM CS 0}}$, $\overline{\text{MEM CS 1}}$, $\overline{\text{MEM CS 3}}$, by NAND gates U21A, U21B, U21C, and U21D, and the two inverters U20B and U20C. The truth table for this conversion is shown in Table 4-12. The chip select signal $\overline{\text{MEM CS 0}}$ is true (LOW) for the first 16 memory locations; then $\overline{\text{MEM CS 1}}$ for the memory locations between 17 - 32, $\overline{\text{MEM CS 2}}$ for memory locations 33 - 48, and $\overline{\text{MEM CS 3}}$ for the memory locations 49 - 64. The timing for the memory address counter is illustrated in Figure 4-17. Test points are provided to monitor the memory address signal MEM ADD 8 (TP1) and the chip select signal $\overline{\text{MEM CS 1}}$ (TP4).

Table 4-12. Chip Select Decoder

MOST SIGNIFICANT MEMORY ADDRESS SIGS		CHIP SELECT SIGNALS			
MEM ADD 16	MEM ADD 32	$\overline{\text{MEM CS 0}}$	$\overline{\text{MEM CS 1}}$	$\overline{\text{MEM CS 2}}$	$\overline{\text{MEM CS 3}}$
LOW	LOW	LOW	HIGH	HIGH	HIGH
HIGH	LOW	HIGH	LOW	HIGH	HIGH
LOW	HIGH	HIGH	HIGH	LOW	HIGH
HIGH	HIGH	HIGH	HIGH	HIGH	LOW

h. A2A7 Recirculating Memory (Logic Diagram Figure A-46, Block Diagram Figure A-35, Wiring Diagram Figure A-73, and Timing Diagrams Figures A-59 and A-64).

(1) XMTR 40 Memory A. - This block consists of 64 memory locations with three data bits stored at each location, or address. The block consists of four 64-bit random access memory modules U15, U16, U17, U18 (Figure A-23), and three pull-up resistors R13, R14, and R15--each 10k ohm. Each memory chip has four memory address signals MEM ADD 1, MEM ADD 2, MEM ADD 4 and MEM ADD 8, which select any one of 16 memory addresses in each chip. In addition, each of the four memory chips is enabled by the active chip select signals MEM CS 0, MEM CS 1, MEM CS 2 or MEM CS 3. Thus the eight memory address control signals select any one of the 64 possible memory addresses. In the A memory 3 data bits are stored at each address, the ARQ cycle marker bit MEM IN 8, the SYNC cycle marker bit MEM IN 9, and the memory parity bit. The memory write signal MEM WRITE A is never inhibited, so that the A memory can be changed at every

character time--even during ARQ and SYNC cycles. The output signals of the A memory are inverted; hence the output for the ARQ marker is MEM OUT 8, for the SYNC marker is MEM OUT 9, and for the parity bit is PARITY BIT. The timing for the memory is illustrated in the timing drawings, Figure A-60 through A-64. The address is changed by the timing signal X PL CLK. The write pulse MEM WRITE A occurs after the timing signal X N CLK (approximately half a bit time later). The output signals MFM OUT 9 and MEM OUT 10 can be monitored at test points TP6 and TP7 respectively.

(2) XMTR 41 Memory B. - This block consists of 64 memory locations with nine data bits stored at each location, or address. The block consists of eight 64- bit random access memory modules U2, U3, U4, U5, U8, U9, U10, and U11 (Figure A-23); one 256- bit random access memory module U21 (Figure A-22); nine inverters U6A, U6B, U6C, U6D, U6E, U6F, U13A, U13E, and U13F; and nine pull-up resistors R3, R4, R5, R6, R7, R8, R9, R10, R12 all 10K ohms. The memory chip U21 has 256 single bit addresses, of which only the first 64 are used; these are defined by the memory address signals MEM ADD 1, MEM ADD 2, MEM ADD 4, MEM ADD 8, MEM ADD 16 and MEM ADD 32. The memory module U21 is used to store the supervisory character marker signal MEM IN 8. The memory chip inverts the data stored. In order to make the output identical to the input, the inserter U13A is employed. Memory chips U2, U3, U4, U5, U8, U9, U10 and U11 have 16 addresses, and four bits stored at each address. The method of selecting any one of 64 memory addresses is identical to that used for memory A, using the four memory address signals MEM ADD 1, MEM ADD 2, MEM ADD 4, and MEM ADD 8, to select any of the 16 addresses on each chip and the four chip select signals MEM CS 0, MEM CS 1, MEM CS 2, and MEM CS 3 to select the active memory chip. The memory chips are arranged in pairs (U2, U8; U3, U9; U4, U10; and U5, U11) to store the eight bits required at each address. The output of the memory is made identical to the input with the eight inverters U6F, U6A, U6D, U6E, U6B, U6C, U13F, and U13E. Normally the incoming data terminal codes are stored in sequential memory address, but when the selected portion of the memory is filled, the next terminal code is stored in the first memory location; the code originally stored there is lost The transmitter actually transmits the encoded constant ratio version of the terminal code at the same time that it is stored in the memory and the memory remembers up to a maximum of 64 terminal codes (characters) that have been transmitted. The memory write signal MEM WRITE B, which changes the terminal codes stored in the memory, is disabled after the second character of an ARQ cycle (the first two characters of an ARQ cycle are always ARQ supervisory characters, and are stored in the memory). With the memory write signal MEM WRITE B disabled, the transmitter retransmits the contents of the memory. The timing for the memory B is identical that of the memory A block; it is illustrated in the timing diagrams (Figures A-60 through A-64). The signals MEM IN 3 and MEM OUT 3 can be monitored at

test points TP2 and TP1 respectively. The memory write signal MEM WRITE B can be monitored at test point TP4.

(3) XMTR 42 Parity Generator. - This block examines the eleven bits to be stored at each address in memory A and memory B and generates a twelfth bit so that the total number of 1's (HIGHs) to be stored is always an odd number (ODD PARITY). The block consists of two parity generators U12 and U19 (Figure A-11), which are cascaded to examine all eleven bits that are to be stored in the memory. The odd input (Pin 3) of the first parity generator U12 is set HIGH by R11, which enables the generator to generate the odd parity signal PARITY BIT IN at the output (Pin 5) U19. The parity signal PARITY BIT IN is HIGH or LOW depending upon the number of HIGH's in the incoming data. The total number of HIGH's stored including the parity bit is always ODD.

(4) XMTR 43 Parity Checker. - This block checks that the twelve bits stored in the memory after a write pulse have odd parity, and lights an indicator on the front panel if the check fails. The block consists of two parity generators U7 and U14 (Figure A-11); two NAND gates U1A, U20A (Figure A-2); two NOR gates U1B, U1D (Figure A-2); and four inverters U1C, U20B, U20C (Figure A-2), U13B (Figure A-1). The complement of the 11-bit memorized signal (which has opposite parity to the memorized signal) is applied to the inputs of the parity checker U14 and U7. The parity bit generated by the parity generator (XMTR 42) and stored in memory A determines the correct parity (ODD or EVEN) for these eleven bits. The parity bit can be monitored at test point TP5; it forms the ODD input (Pin 3) for U14 and its complement forms the EVEN input (Pin 4). The parity checkers U14 and U7 are cascaded, and the output (Pin 5) of U7 is LOW if the output signals form the memory have correct parity. This signal can be monitored at test point TP3. NOR gates U1B and U1D form an R-S flip-flop which, when set, generates the signal PAR FAIL IND FP via the lamp driver U1C and lights the PARITY FAIL indicator on the front panel. The flip-flop is reset directly by the parity fail reset signal PAR FAIL RES generated by the front panel reset PARITY FAIL switch. The memory output signals are checked for correct parity by the timing signal X L PS CLK, which occurs 3 microseconds after the memory write signal enabling the NAND gate U1A, via gates U20C, U20A, U20B. The parity check is disabled during an ARQ cycle by NAND gate U20A and the control signal MEM ARQ INH.

4-15. **AN/FYC-12 RECEIVER. - This section describes the overall functions of the receiver; the logic functions of each block are described in detail to enable a proper understanding of the receiver operation. Reference is made throughout the following discussion to the appropriate top level and subsystem block diagrams, and the receiver timing diagrams. The AN/FYC-12 receiver performs the task of receiving input data via a low level (MIL STD 188C) transmission circuit using a special constant ratio character code, then validating each character and decoding the received data to the original standard character codes as received by the distant transmitter. In addition, the receiver must respond to certain control characters called Supervisory characters, which may request a retransmission of data (ARQ), halt the local transmitter (Inhibit Activate), or resynchronize the local receiver to incoming data (Sync A and Sync B). The logic components for the AN/FYC-12 receiver are contained on four circuit boards:**

1. A2A8 Level Converter
2. A2A9 RCVR Data Processor
3. A2A10 RCVR Control Logic
4. A2A11 RCVR ARQ and SYNC Control

To help understand the complex logic, the functions of each circuit card are reduced to logical blocks, which are described in detail. The logical blocks for the receiver circuit boards are:

1. A2A8 Level Converter (Figure A-36)
   a. RCVR 1 Incoming Data Line Receiver
   b. RCVR2 Receiver Clock Line Receiver
   c. RCVR 29 Receiver Clock Step Line Driver
   d. RCVR 30 Mutilated Character Indicator Line Driver
   e. RCVR 31 Outgoing Data Line Driver
2. A2A9 RCVR Data Processor (Figure A-37)
   a. RCVR 12 Data Input Timing
   b. RVCR 13 Mutilated Code Detector
   c. RCVR 14 Serial-To -Parallel Converter
   d. RCVR 15 Supervisory Character Decoder
   e. RCVR 16 Unused Constant Ratio Code Detector
   f. RCVR 17 Constant Ratio Code Decoder

g. RCVR 18 Parallel-To-Serial Converter

h. RCVR 19 Data Inhibit

3. **A2A10 RCVR Cont Logic (Figure A-38)**

a. RCVR 3 Test Normal Mode

b. RCVR 4 **RCVR Clock Generator**

c. RCVR 5 **RCVR Bit Counter**

d. RCVR 6 **Test Unsync A**

e. RCVR 7 Test Unsync B

f. RCVR 8 ARQ Counter Skip In Re-Sync

g. RCVR 9 Block Step Generator

h. RCVR 10 Data Inhibit Control

i. RCVR 11 Data Timing

4. A2A11 RCVR ARQ and SYNC Cont (Figure A-39)

a. RCVR 20 Mutilated Character Indicator

b. RCVR 21 Synchronizing Pattern Detector

c. RCVR 22 Two Supervisory ARQs Received

d. RCVR 23 Initialize ARQ and SYNC Converter

e. RCVR 24 ARQ Cycle Counter

f. RCVR 25 SYNC Cycle Counter

g. RCVR 26 ARQ Flag

h. RCVR 27 Inhibit Flag

i. RCVR 28 Sync Flag

The following is a description of each logic block, starting with the first block on Level Converter A2A8. The function of the logic is detailed; then a signal by-signal description is given. It will be helpful to refer to the Receiver Signal Name Glossary (Table 6-3) and the applicable circuit board logic diagram.

a. A2A8 Level Converter (Logic Diagram Figure A-43 Block Diagram Figure A-36, Wiring Diagram Figure A-74). -

(1) RCVR 1 Incoming Data Line Receiver. - This block converts the incoming bipolar (MIL STD 188C) low level interface signal into a TTL com-

patible signal. The conversion is accomplished by an integrated circuit. Dual Interface Receiver U3, which is described in Figure A-13. The incoming data signal R IN DA L and its return R IN DA LR is converted into the TTL Signal $\overline{\text{R IN DA}}$. The output signal is inverted; test point TP3 is provided for monitoring.

(2) RCVR 2 Receiver Clock Line Receiver. - This block converts the incoming receiver clock signal (which is derived from the incoming data, is at twice the data rate, and phased so that the fall of the clock is at the center of each data bit) from a bipolar to a TTL compatible signal. It can be seen from Figure A-47 that the same integrated circuit Dual Interface Receiver U3, used for incoming data conversion, is also for the receiver clock conversion. The incoming receiver clock signal R CLK L and its return R CLK LR is converted into the TTL Signal $\overline{\text{R CLK}}$, which is also inverted. The receiver clock signal $\overline{\text{R CLK}}$ can be monitored at test point TP2.

(3) RCVR 29 Receiver Clock Step Line Driver. - This block converts the TTL receiver clock step signal into a bipolar (MIL STD 188C Low level interface) signal. The conversion (including voltage and current limiting required by the specification) is accomplished by an integrated circuit, Dual Interface Transmitter U5, which is described in Figure A-12. The waveshape of the output signal is controlled by the discrete capacitor C9, the capacitance of which depends upon the baud rate in use. The factory-installed value of C9 is 0.0033 μF; this is the value for the highest baud rate--9600 baud. The TTL clock signal R CLK ST is converted to the bipolar signal R CLK ST L with a common return line OUT SIG RTN. Figure A-47 shows that the TTL signal R CLK ST is also inverted by the line driver and that a test point TP5 is provided for monitoring the bipolar output signal.

(4) RCVR 30 Mutilated Character Indicator Line Driver. - This block converts the TTL mutilated character signal into a bipolar (MIL STD 188C) low level interface signal suitable for transmission to the data control room. The same type of integrated circuit used for the receiver clock step (Figure A-12) is used; the waveshape capacitor is C11, The TTL signal MC IND is converted into the bipolar (MIL STD 188C) signal MC IND L with common return line OUT SIG RTN.

(5) RCVR 31 Outgoing Data Line Driver. - This block converts the TTL data signal into a bipolar (MIL STD 188C) level interface signal suitable for transmission to the data sink terminal. It uses the same type of integrated circuit as the receiver clock step (Figure A-12); capacitor C10 is used for wave shaping. The TTL data signal R O DA B is converted into the bipolar outgoing data signal.

b. A2A9 RCVR Data Processor (Logic Diagram Figure A-48, Block Diagram Figure A-37, Wiring Diagram Figure A-75, Timing Diagrams Figures A-65, A-66).

(1) RCVR 12 Data Input Timing. - The function of this block is to clock the incoming data at the center of each bit time. The receiver clock is derived from the incoming data, is at twice the data rate, and is phased so that the data changes at the rise of the clock (Figure A-66). Thus the fall of the receiver clock is always at the center of each data bit time, and can be used to clock the incoming data at the correct time. The serial input data signal R IN DA from RCVR 3 (Test Normal Mode block) is applied to the D input (Pin 2) of flip-flop U4A (Figure A-14), which is clocked by the inverted receiver clock signal $\overline{\text{R CLK}}$. Therefore, the D type flip-flop U4A can change state only at the rise of $\overline{\text{R CLK}}$ (the fall of the receiver clock). Therefore, the incoming data is clocked at the center of each data bit time. The output signals from this block are R IN DA DL and its complement $\overline{\text{R IN DA DL}}$, which are used by the serial-to-parallel converter (RCVR 14) and the mutilated character detector (RCVR 13). The signal R IN DA DL can be monitored at test point TP7.

(2) RCVR 13 Mutilated Character Detector. - The function of this block is to count the number of 1's in each incoming character code. Every constant ratio code transmitted has four 1's, If more or less than four 1's are detected in any one character, an error in transmission is indicated. The mutilated character detector consists of a 4-bit synchronous counter U16 (Figure A-18), a J-K flip-flop W23A (Figure A-16), two two-input NAND gates U22C and U22D (Figure A-2), and three inverters U22A and U22B (Figure A-2), and U18A (Figure A-1). The counter U16 is loaded by the rise of R N 1 CLK during receiver last bit time R BIT LAST true (LOW) with a count of 11 (Binary 1 0 1 1). This count is always present at the load inputs A, B, C, D, of counter U16. Thus, at the end of every character (assume that the receiver is synchronized to incoming data) the counter U16 is loaded with a count of 11; four more counts are required to generate a carry at C O (Pin 15). (This occurs with a count of 15.) Referring to the logic diagram (Figure A-48) the carry signal called NCR RCVD forms the output of this block; if it is true (LOW) at the end of a received character--R BIT LAST true (HIGH) --then a non -constant ratio character code has been received. The counter U16 is enabled to count at R N 1 CLK time by the output of U22D (Pin 11), which is connected to the enable input (Pin 7) of the counter. The gate U22D forms a negative logic NOR function; that is, if either inputs (Pin 12 or Pin 13) are LOW, the counter is enabled. The first Input (Pin 12) is connected to the output of data input timing block (RCVR 12) signal R IN DA DL, and is true (LOW) when the incoming data is HIGH, or when a 1" has been received. Thus, counter U16 is enabled when the incoming data R lN DA DL is HIGH or a logic 1 is received, If the first bit of a new character code is a logic 1 (HIGH), the counter (U16) loads a count of 11 at R N1 CLK time and

the first 1 of the constant ratio code is lost. The memory element (J-K flip-flop U23A) checks the first bit of any constant ratio code. The two-input NAND gate U22C and inverter U22A form a two-input AND gate. Pin 9 of U22C looks at the incoming data signal R IN DA DL. Pin 10 is enabled at last bit time by R BIT LAST, generated from R BIT LAST by U18A. The memory element U23A is clocked at the same time as the counter U16 by R N1 CLK generated from $\overline{\text{R N1 CLK}}$ by inverter U22B; if J input (Pin 1) is set HIGH, the memory element is set; Q (Pin 3) becomes HIGH and $\overline{\text{Q}}$ (Pin 2) becomes LOW, but the counter U16 is loaded at a count of 11. Thus, if the first bit of the constant ratio code received is a 1, memory element U23A is set and the counter U16 is loaded as usual with a count of 11. If the second bit is also a 1, $\overline{\text{R IN DA DL}}$ (which is true (LOW) because it is connected to the K input (Pin 4) of memory element U23A) causes both K and J inputs to be LOW and the memory element remains set. The counter is enabled by Pin 12 of U22D and adds one count. This procedure is repeated until the data bit received is a logic 0, and $\overline{\text{R IN DA DL}}$ is HIGH forcing the K input (Pin 4) of U23A HIGH which resets the memory element (U23A) on the next clock pulse. The counter U16 remains enabled by Pin 13 of U22D and adds one count to correct for the first logic 1, which was omitted. The only output signal of the mutilated character detector (RCVR 13), is $\overline{\text{NCR RCVD}}$, monitored at test point TP8, This signal is valid only at the end of each character examined during last bit time of the receiver. The complete timing for clocks and data bit times is illustrated in Figure A-65, Receiver 8-Bit Code Format Bit Timing, and A-66, Receiver 11-Bit Code Format Bit Timing as shown, R N1 CLK occurs after the fall of R CLK near the center of every data bit time and is half the fast clock (3 µsecs) in width. The receiver last bit time occurs during the last half of last data bit time and the first half of the first data bit time and is timed by the trailing edge of R N1 CLK. The absolute last bit time depends upon the data baud rate and is approximately the period of the receiver clock signal R CLK.

(3) RCVR 14 Serial-To-Parallel Converter. - The function of this block is to convert the incoming serial data into parallel words, either 8 Bits or 11 Bits wide dependent upon format. The input signal R IN DA DL is the serial input data from the Data Input Timing block (RCVR 12); the eleven output signals R CODE 0 through R CODE 10 form the constant ratio code for the character received. The serial-to-parallel converter consists of an 11-Bit shift register made up of U9 (Figure A-21) 8-Bit parallel-out serial-in shift register and U11 (Figure A-20) 4-Bit parallel-access shift register cascaded together to make up the required 11 bits; the last bit from U11 is not used. In 8-Bit constant ratio code formats the last 3 Bits are held LOW at all times (the control signal CODE 11 BIT is false (LOW) and resets shift register U11 by holding reset (Pin 1) LOW). Referring to the logic diagram (Figure A-48), the last output bit QH (Pin 13) of U9 is connected to input (Pin 2 and Pin 3) of U11 to form the 11 bit shift register. The register is clocked by R N1 CLK, which occurs at the center of every data bit (see re-

ceiver timing diagram Figure A-65). Therefore, at receiver last bit time, which occurs after 8 or 11 clocks of the shift register, the output lines R CODE 0 through R CODE 10 contain (in parallel) the constant ratio code of the character just received. These lines are constantly changing as the serial data bits are shifted through; the register is not reset between characters.

(4) RCVR 15 Supervisory Character Decoder. - The function of this block is to generate output signals IDLE RCVD, ARQ RCVD, INH ACT RCVD, INH DEACT RCVD, SYNC A RCVD, SYNC B RCVD and SYNC 0 RCVD when supervisory characters are recognized on the parallel output lines R CODE 0 through R CODE 10 from serial-to-parallel converter block (RCVR 14). The system control supervisory characters are the same in both formats and need only be recognized at receiver last bit time. Since the receiver is in character synchronization with the incoming data. The two synchronization supervisory characters must be recognized at any bit time, for when received, the receiver must be assumed to be out of character synchronization. The synchronization supervisor transmitted is always SYNC A followed by SYNC B, generating eight sequential 1's followed by four or seven 0's, a sequence that can be recognized by the receiver at any bit time. Consider first the control supervisory characters IDLE, ARQ, INH DEACT and INH ACT. As shown in Table 4-6, they are the same in both 11- and 8-bit constant ratio formats except for the leading three zeroes in the 11- bit format. R CODE 3 (The fourth bit)is HIGH for all four control supervisory characters. The NAND gate U24A and inverter U24D form a logical AND function. The fourth bit of the constant ratio code R CODE 3 is connected to U24A (Pin 1) and the non-constant ratio code signal NCR RCVD is connected to Pin 2 of the same gate. Thus, the output of inverter U24D (Pin 11) and the test point TP4 is HIGH during receiver last bit time providing the fourth bit of the constant ratio code is 1 (HIGH) and that only four 1's have been received during the character time (True constant ratio code received). In or&r to fully decode the four control supervisory characters it is only necessary to locate the position of the three remaining 1's, Thus four NAND gates U1A, U1B, U2A and U2B are used to decode IDLE, ARQ, NH DEACT, and INH ACT respectively. The outputs of these four gates generate the signal IDLE RCVD, ARQ RCVD, INH DEACT RCVD and INH ACT RCVD which are true (LOW) at last bit time if the control supervisory character is on the data lines. Now consider the two synchronizing supervisory characters SYNC A and SYNC B, which must be detected at any time. The final decision on the reception of SYNC A followed by SYNC B is made by the SYNC Pattern Detector block (RCVR 21) on circuit board A2A11. The supervisory character decoder uses U8A to determine if four consecutive data l's are on lines R CODE 10, R CODE 9, R CODE 8 and R CODE 7. If so, it's output (Pin 6) is the LOW and SYNC A RCVD is true (LOW). This does not mean that the synchronizing supervisory character has been received, only that the four consecutive k's may be the first of the eight required. As shown in Table 4-6 SYNC A is

the same in both 11 and 8 Bit constant ratio code formats, but SYNC B (being the first four bits transmitted) depends upon format. The two-input NAND gate U20D looks at the only common line, R CODE 3, (the fourth bit, on input Pin 13), which must be HIGH in both 11- and 8-bit formats. The data lines R CODE 4, R CODE 5, and R CODE 6 are tested for all 1's by NAND gate U8B and enabled when control signal CODE 8 BIT is true (HIGH) (in 8-bit constant ratio code format R CODE 0, R CODE 1, and R CODE 2, are all permanently LOW because of the reset on register U11. The output of U8B (Pin 8) is logically AND'ed to R CODE 3 via negative logic NOR gate U20C and NAND gate U20D. The output of U20D (Pin 11) generates output signal SYNC B RCVD true (LOW) when R CODE 4, R CODE 5, R CODE 6 and R CODE 3 are all HIGH at the same time. In the 11- bit constant ratio code format U8B is disabled because CODE 8 BIT is false (LOW) putting a LOW on the input (Pin 10) and forcing the output (Pin 8) to be HIGH at all times. The NAND gate U19A tests R CODE 0, R CODE 1 and R CODE 2 for all 1's and ANDs the result via negative logic NOR gate U20C and NAND gate U20D. The output signal SYNC B RCVD is true (LOW) when R CODE 0, R CODE 1, R CODE 2, and R CODE 3 are all HIGH, which is the requirement for SYNC B in the 11- Bit constant ratio code. The last output $\overline{\text{SYNC 0 RCVD}}$ is determined by three of the following 0's required for a true SYNC B to be received. The signals R CODE 7, R CODE 8 and R CODE 9 are inverted in un-used code detector (RCVR 16) into $\overline{\text{R CODE 7}}$, $\overline{\text{R CODE 8}}$, $\overline{\text{R CODE 9}}$ then NANDed by U19B to produce $\overline{\text{SYNC 0 RCVD}}$ at the output Therefore, SYNC 0 RCVD is true (LOW) when R CODE 7, R CODE 8 and R CODE 9 are all LOW--in any format. The output signals SYNC A RCVD, SYNC B RCVD and SYNC 0 RCVD are tested in receiver block A2A11 (RCVR 21) Sync Pattern Detector for a true resynchronization pattern of SYNC A followed by SYNC B.

(5) RCVR 16 Unused Constant Ratio Code Detector. - The function of this block is to detect all constant ratio codes that are not used in the selected format and must therefore have been mutilated in transmission, The block generates the output signal $\overline{\text{UN USED RCVD}}$ which if true (LOW) at last bit time indicates that an unused constant ratio code has been received, The block consists of seven NAND gates U14B, U14C, U14D, U20A, U24C (Figure A-2), U17 (Figure A-8), and U21A (Figure A-4); Six NOR gates U14A, U20B, U24B (Figure A-2), U19C, U21C (Figure A-4), U7A (Figure A-6); and twelve inverters U13A, U13B, U13C, U15A, U15D, U15E, U15F, U18B, U18C, U18D, U18E, U18F (Figure A-1).

(a) ln the 11- bit constant ratio code format there are 68 constant ratio codes always declared unused. The control signal CODE 11 BIT is true (HIGH) for all 11- Bit constant ratio code formats and enables NAND gate U21A at input (Fin 13). U21A examines the data signal R CODE 9 (generated from R CODE 9 by inverter U15E) and the output of negative logic NOR gate U20B, which logically OR's the outputs of NAND gates U17 and U20A. The

output of the NAND gate U20A is active (LOW) when the data signal R CODE10 and the output of negative logic NOR gate U19C are both HIGH. This occurs when any of the data signals R CODE 0, R CODE 1, R CODE 2 are HIGH (the signals are inverted by U18D, U18E, and U18F, and logically OR'ed by negative logic NOR gate U19C). From this it follows that, if R CODE 10 is HIGH, and R CODE 9 is LOW, any of the data signals R CODE 0, R CODE 1 or R CODE 2 can not be HIGH for a valid constant ratio code. This logic invalidates 64 of the 11- bit constant ratio codes that are never transmitted and, if received, must be the result of a transmission error. The output of NAND gate U17 declares four more 11 bit constant ratio codes always unused. NAND gate U17 examines R CODE 6, R CODE 5, R CODE 4, R CODE 10, R CODE 8, and R CODE 7 (the inverted signals generated by inverters U15D, U15F and U15A). R CODE 9 is also logically AND'ed to the final output by NAND gate U21A. Thus if R CODE 6, R CODE 5, and R CODE 4 are all HIGH, the remaining HIGH for an 11- bit constant ratio code can not be R CODE 3, R CODE 2, R CODE 1, or R CODE 0 for a valid constant ratio code. This logic invalidates four more 11- bit constant ratio codes, including the 8- bit SYNC B supervisory character, making a total of 68 11- bit constant ratio codes that are always declared unused by the output of NAND gate U21A--which can be monitored at test point TP6. The output signal is only valid during the last bit time when the complete constant ratio code is on the data lines. The total number of 11- bit constant ratio codes is 330, of which 68 have been declared unused, leaving 262 valid 11- bit constant ratio codes for all incoming data characters.

(b) In 8- bit start-stop data format there are 256 data characters, and 6 supervisory control characters, making a total of 262 different character codes. Therefore, in 8- bit start-stop data format all the available 11- bit constant ratio codes are used.

(c) In 7- bit start-stop data format there are only 128 data characters, and the same 6 supervisor characters, making a total of 134 different character codes--leaving 128 11- bit constant ratio codes unused. In this format the start bit, which is always LOW, is considered part of the incoming data terminal code making up an 8- bit code that is encoded into an 11- bit constant ratio code. The unused logic examines the first bit (start bit) after the consta.. ratio code has been decoded back to the original data codes; for a valid constant ratio code this bit must be LOW. This invalidates another 128 11- bit constant ratio code by making the output of NAND gate U14C LOW if the first bit of the data terminal code is not a valid start bit (LOW). NAND gate U14C is enabled by the control signal 7 BIT S-S, which is generated from the signal $\overline{7\ \text{BIT S-S}}$ by inverter U13E. The other input of NAND gate U14C is the data signal R BIT 7 (start bit in this mode); if HIGH, it enables NAND gate U14C, and its output (Pin 8) goes LOW generating an unused character signal.

(d) In 6-bit start-stop data format there are only 64 data characters, and the same 6 supervisory characters, making a total of 70 different characters--leaving 192 unused 11-bit constant ratio codes. In this format the start bit (always LOW) is also included as part of the incoming data terminal code and the leading bit of the pseudo-8-bit incoming terminal code is forced HIGH (stop bit) so that the first bit is always HIGH, the second bit is always LOW, and the six data bits follow. The unused logic examines the first two bits after the constant ratio code has been decoded. For a valid constant ratio code the first bit must be HIGH and the second bit must be LOW. This invalidates 192 11-bit constant ratio codes by making the output (Pin 11) of the NAND gate U14D LOW, if the above conditions are not true. NAND gate U14D is enabled by the control signal 6 BIT S-S, generated from 6 BIT S-S by inverter U13D. The other input is NAND gate U14D is the output of negative logic NOR gate U14A, which logically OR's R BIT 7 and R BIT 6, Thus, for the output of NOR gate U14A to be LOW for a valid character R BIT 7 must be HIGH and R BIT 6 (start bit in this mode) must LOW. If not, NAND gate U14D output pin 11) goes LOW, generating an unused character signal.

(e) In S-bit start-stop data format there are only 32 data characters, and the same 6 supervisory characters, making a total of 38 different characters. In this mode the 8-bit constant ratio code is used, which has only 70 available combinations. NAND gate U21A is disabled by the control signaI CODE 11 BIT being false (LOW), which disables the 68 character unused logic for the 11-bit constant ratio codes. Therefore in S-bit start-stop data format there are 32 unused 8-bit constant ratio codes. As in the other formats the start bit is included with the data bits and the two leading bits of a pseudo-8-bit incoming terminal are also forced LOW so that the first three bits of the data code are always LOW, followed by the five data bits. The unused logic examines the first three bits after the constant ratio code has been decoded, For a valid constant ratio code they must all be LOW. This invalidates 32 of the 8-bit constant ratio codes by making the output (Pin 6) of NAND gate U14B LOW. NAND gate U14B is enabled by the control signal 5 BIT S-S generated from 5 BIT S-S by inverter U13C. The other input of the negative logic NOR gate U21C, which logically OR's R BIT 5, R BIT 6, and R BIT 7. Thus for the output of the NOR gate U21C to be LOW for a valid character R BIT 5, R BIT 6, and R BIT 7 must all be LOW (R BIT 5 is the start bit in this mode). If not, NAND gate U14B output (Pin 6) goes LOW, generating an unused character signal.

(f) In bit stream data format there are 64 data combinations and 6 supervisory characters, making a total of 70 different combinations, which is the total number of 8-bit constant ratio codes --leaving none unused.

(g) The unused signals in the different data formats are logically OR'ed by the negative logic NOR gate U7A. The common output can be moni-

bored at test point TP5. The six supervisory characters are not decoded with a start bit in the correct position, and are considered unused constant ratio codes. NAND gate U24C disables the unused logic if any of the six supervisory characters are decoded by the supervisory character-decoder (RCVR RCVR 15). The signal SUPER RCVD is generated by the data inhibit control block (RCVR 10) and is the logical OR of the signals ARQ RCVD, INH ACT RCVD, INH ACT RCVD, INH DEACT RCVD, SYNC A RCVD and SYNC B RCVD. This signal is logically ORed to the supervisory signal IDLE RCVD by negative logic NOR gate U24B, the output of which (Pin 6) is HIGH if any of the six supervisory characters are received. This disables NAND gate U24C via inverter U18C. Therefore, for a character to be declared unused at the output of the NAND gate U24C, it can not be one of the six supervisory characters.

(6) RCVR 17 Constant Ratio Code Decoder. - The function of this block is to convert the incoming constant ratio codes back to the original data codes received by the distant transmitter. (The AN/FYC-12 is code transparent in all formats: the receiver output is identical to the transmitter input). The constant ratio code decoder consists of two 256-address 4 bit wide read only memories U10 (Figure A-24A) and U12 (Figure A-248). Referring to the logic diagram (Figure A-48) the output data lines--R Code 0 through R Code PO-- of Serial-To-Parallel Converter RCVR 14 form the composite address for the two ROM's, which have been programmed to decode each input address (constant ratio code) into the correct 8-bit data code. The eight output signals R BIT 0 through R Bit 7 require pull-up resistors R3, R4, R5, R6, R8, R9, R10 and R11 and the programming is such as to make them true signals. The first bit to be transmitted is R BIT 7.

(7) RCVR 18 Parallel-To-Serial Converter. - The purpose of this block is to convert the parallel output of the Constant Ratio Code De-coder into a serial output stream formatted correctly, with start and stop bits added as required by the selected format. The parallel-to-serial converter consists of a 9-Bit parallel-load shift register consisting of U3 (Figure A-20), U5 (Figure A-20) and U4B (Figure A-14) cascaded together to form the 9-Bit configuration. The register is parallel loaded during receiver last bit time by R N2 CLK, which from the timing diagram (Figure A-65) occurs one fast clock period (6 µsec) after R N1 CLK. The constant ratio data lines R CODE 0 through R CODE 10 and ROM logic have 6 microseconds to settle before being loaded into the parallel-to-serial shift register by R N2 CLK. Referring to the logic diagram (Figure A-48) the Shift Load terminal (Pin 9) on U3 and U5 is held active (LOAD) by the R BIT LAST timing signal and U4B (which generates the start bit in 8-bit start-stop format) is reset by the same signal. At the rise of R N2 CLK a new character code is parallel loaded into the shift register (U3 and U5), which is shifted one bit by each of the following R N2 CLK pulses. Logical l's are entered into U3 and U5 as the terminal code is shifted out, since the J-K inputs (Pins 2 and 3) of U3 are held

HIGH by R2. This sends a stop bit (always HIGH) in all start-stop formats. The numbers of bits serially sent to the data terminal depends upon the data format selected. NAND gates U6A, U6B, U6C, and U6D are used to select this format.

(a) In 8-bit start-stop the gate U6B is enabled by control signal 8-BIT S-S generated from 8 BIT S-S by the inverter U13F, Thus, the output of Q (Pin 9) on U4B is the first bit sent. U4B was reset at the last bit time; hence, the first bit sent is LOW and becomes the start bit. Eight data code bits follow at every R N2 CLK time, followed by two HIGH's (stop bits) making up the eleven bit times available.

(b) In 7-bit start-stop the gate U6A is enabled by control signal 7 BIT S-S generated from 7 BIT S-S by the inverter U13E. The first bit sent is therefore the QD (Pin 12) on US, which in 7-Bit start-stop format is always LOW, forming the start bit. Seven data code bits follow at every R N2 CLK time, followed by three HIGH'S (Stop Bits) making up the eleven bit times available.

(c) In 6 Bit Start-Stop the gate U6D is enabled by control signal 6 BIT S-S generated from 6 BIT S-S by the inverter U13D. In this case the first bit sent is QC (Pin 13) on U5, which in 6 Bit-start-stop format is always LOW, forming the start bit. Six data code bits follow at every R N2 CLK time, followed by four HIGH'S (Stop Bits) making up the eleven bit times available.

(d) In S-bit start-stop and bit stream mode U6C is enabled by the control signal CODE 8 BIT; the first bit sent is from QB (Pin 14) of U5, which in 5 bit start-stop format is always LOW, forming the start bit. Five data code bits follow at every R N2 CLK time, followed by two HIGH'S (stop bits) making up the eight bit times available in this format. In the bit stream mode six data bits are transmitted, followed by two HIGH'S; a data clock step is provided to synchronize the bit stream data terminal sink. The negative logic NOR gate U7B combines the outputs of U6A (Pin 3) U6B (Pin 6), U6C (Pin 8) and U6D (Pin 11) to form the serial data output from this block R O DA.

(8) RCVR 19 Data Inhibit. - The function of this block is to inhibit the flow of serial data when any supervisory character is received, or when the system is in an ARQ or SYNC cycle. The serial data signal R O DA is inverted by inverter U15B (Figure A-1) and applied to (Pin 3) of the NAND gate U21B (Figure A-4), which is enabled by control signal R CUT EN and R IDL DA INH; both must be HIGH to enable data to reach the data sink. The output of this block is named R O DA A, and can be monitored at test point TP3.

c. A2A10 RCVR Cont Logic (Logic Diagram Figure A-49, Block Diagram Figure A-38, Wiring Diagram Figure A-76, Timing Diagram Figure A-65, A-66). -

(1) RCVR 3 Test/Normal Mode. - The purpose of this block is to enable the local transmitter to be looped to the local receiver as an aid to troubleshooting, The receiver clock signal R CLK is also looped to the transmitter clock signal X CLK 1, and the system is forced out of character synchronization. The Test Normal Mode block consists of two AND-OR INVERTER U1A and U1B (Figure A-9), inverter U3C (Figure A-1) and a J-K flip-flop U7A (Figure A-15). The control signals TEST and TEST are generated from the TEST switch on the front panel; TEST is true (HIGH) when the Test Mode is selected, The four input signals that are switched by this block are R IN DA (the normal receiver data input), SND LIN (the local transmitter output signal) R CLK (the receiver timing clock generated from the incoming data), and X CLK 1 (the local transmitter timing clock). The two output signals of this block are R IN DA (the input data signal for the receiver), and R CLK (the actual receiver timing signal). When Test Mode is selected, the signal TEST becomes true (LOW); it is inverted by U3C and applied as the J input (Pin 14) of J-K flip-flop U7A. At the fall of the transmitter timing signal X CLK 1 the flip-flop is SET, causing Q (Pin 12) to be HIGH and Q (Pin 13) to LOW. Referring to the logic diagram (Figure A-49) Q (Pin 12) of U7A is connected to (Pin 4) of U1A; it enables the transmitter signal SND LIN to become the receiver input signal R IN DA. Q (Pin 12) is also connected to (Pin 9) of U1A, and enables the transmitter timing signal X CLK 1 to become the receiver timing signal R CLK. In the Normal Mode the J-K flip-flop U7A is reset by controlsignal TEST becoming false (LOW). The reader can easily follow the operation of switching gates U1A and U1B. The output signals of J-K flip-flop U7A-Q and Q- are also used by the UNSYNC blocks (RCVR 6) and (RCVR 7) to force an error in the character synchronization, when the Test Mode is selected.

(2) RCVR 4 RCVR Clock Generator. - The function of this block is to generate the required timing signals for the correct operation of the receiver logic. The block uses the receiver clock signal R CLK and the fast clock (153.6 kHz) generated by the transmitter Fast Clock Generator (XMTR 12) to generate the receiver timing signals R N1 CLK and R N2 CLK; it also logically AND's them to the receiver last bit time to obtain R L N2 CLK and R L N1 CLK. The fifth timing signal generated is simply the receiver clock inverted, R CLK 1.

(a) The RCVR Clock Generator block consists of three D-type flip-flops U19B, U18A, and U18B (Figure A-14), four NAND gates U17A, U17B, U17C (Figure A-6), and U15C (Figure A-5), and three inverters U12A, U12B (Figure A-1) and U2D (Figure A-2). To understand the operation of this block, refer to the receiver timing diagram (Figure A-65) and the logic

diagram (Figure A-49). From the logic diagram it is clear that the three D-type flip-flops U19B, U18A and U18B are all clocked from the fast clock signal FAST CL-K; they are connected as a shift register. The receiver timing signal R CLK 1 is applied as the input of this shift register at the D input (Pin 12) of U19B and is shifted through U19B, U18A, and U18B, with three periods of the fast clock each 6 microseconds long. Consider the operation of the timing generator from the time that the receiver timing signal R CLK 1 goes LOW. All the flip-flops in the shift register are set (Q HIGH) because R CLK 1 was previously HIGH. On the rise of the FAST CLK signal the first flip-flop U19B is reset, causing the output Q (Pin 8) to go HIGH; this is connected to input (Pin 4) of 3 input NAND gate U17B. Input (Pin 5) is connected to Q (Pin 5) of U18A and is also HIGH; when the FAST CLK signal goes LOW, its complement FAST CLK goes HIGH. This is connected to the third input (Pin 3) of U17B for one half of the fast clock period (3 microseconds) the output of U17B (Pin 6) goes LOW, generating the signal R N1 CLK. At the next rise of FAST CLK the second flip-flop in the shift register -U18A- is reset, causing the output Q (Pin 5) to go LOW, disabling NAND gate U17B; output Q (Pin 6) goes HIGH, enabling NAND gate U17C to generate R N2 CLK upon the fall of FAST CLK in the same manner as R N1 CLK was generated by U17B. At the third rise of FAST CLK the last flip-flop U18B is reset disabling NAND gate U17C. On the rise of the receiver timing signal R CLK 1 no pulses are generated.

(b) The output signal R N1 CLK is logically AND'ed to the receiver last bit time by the negative logic NAND gate U15C. Its output (Pin 8) is the timing signal R L N1 CLK.

(c) The output signal R N2 CLK is inverted by U2D and logically AND'ed to the receiver last bit time by the NAND gate U17A. Its output (Pin 12) is the timing signal R L N2 CLK. Because the R BIT LAST signal is generated by the trailing edge of R N1 CLK, the last clock R L N2 CLK is at the beginning of the receiver last bit time, followed by R L N 1 CLK at the end of the last bit time.

(d) The final output of this block is generated by inverting the receiver timing signal R CLK 1 in U12B (Figure A-1) to produce R CLK 1.

(e) Test points are provided for convenient monitoring of the clock signals. They are:

TP2	R N1 CLK
TP4	R N2 CLK
TP5	R L N2 CLK
TP7	R BIT LAST

(3) RCVR 5 RCVR Bit Counter. - The function of this block is to deter - mine receiver bit timing. The number of bits in each character depends upon the constant ratio code format, either 8 or 11, and relative bit positions (BIT 1, BIT2 . . . LAST BIT, with respect to real time) depends upon the character synchronization. Hence, this block is used to resynchronize the receiver timing to the incoming data during a sync cycle.

(a) The RCVR Bit Counter block consists of a 4-bit binary counter U16 (Figure A-18), two NAND gates U9A, U10A (Figure A-4), a NOR gate U8B, and inverter U2A (Figure A-1). The counter U16 is permanently enabled (Pin 9 and 10 always HIGH) and is initially reset by initialization signal INIT 1-1. It is clocked every bit time by R N1 CLK and therefore counts bit times. In the 8-bit constant ratio code format, NAND gate U9A is enabled by the control signal CODE 8 BIT on input (Pin 5); the other inputs are connected for a count of 7 on the counter U16. Thus, at a count of 7 (the eighth bit) the input of U9A is four 1's and its output (Pin 6) is LOW. This signal is one of the inputs to the negative logic NOR gate U8B, which inverts it to produce the timing signal R BIT LAST; this is again inverted, by U2A and becomes the output signal R BIT LAST. The signal R BIT LAST, which is true (LOW) at the receiver last bit time, is also connected to the load enable (Pin 9) of the counter U16, Thus, on the next R N1 CLK pulse the counter is loaded with the parallel inputs A, B, C, and D (which are all permanently set for O's) so that the counter is reset.

(b) In the 11-bit constant ratio code format NAND gate U10A is enabled by the control signal CODE 11 BIT on input Pin 13. The other inputs are connected for a count of 10 on the counter U16. Thus at a count of 10 (the eleventh bit) the input of U10A has three 1's and its output (Pin 12) goes LOW. This signal is also one of the inputs to the negative logic NOR gate U8B and hence generates the R BIT LAST and R BIT LAST timing signals. The input signal R RESYNC is true (LOW) at the correct last bit time during a SYNC CYCLE. It forces the bit counter into correct synchronization by generating a new load at R N1 CLK time, The remaining input to NOR gate U8B on (Pin 1) is FORCE RCVR LAST BIT, which forces the receiver out of correct synchronization when the system enters the test mode.

(4) RCVR 6 UN-SYNC A. - The purpose of this block is to prevent transmitter and receiver character synchronization when the system is placed in the test mode. The Un-Sync A block consists of three flip-flops U14A (Figure A-14) U5B (Figure A-15) and U21A (Figure A-14), a data latch U21B (Figure A-16), two NAND gates U16B (Figure A5), U6C (Figure A-4), and an inverter U15A (Figure A-5). From the logic diagram (Figure A-49) shows 'the three flip-flop connected as a 3-Bit shift register. Flip-flop U5B (Figure A-15) requires an inverted clock because it changes state on the fall, whereas U4A and U21A change state on the rise of the clock. The rise occurs once per bit at R N 1 CLK time.

(a) The logic is initialized by signal INIT 1 and INIT 1-1 which reset flip-flops U4A and U5B and presets flip-flop U21A (which resets the data latch U21B). When the system enters the Test Mode flip-flop U7A (RCVR 3) is preset and its output Q (Pin 13) goes LOW; this LOW signal is connected to the K input of J-K flip-flop U5B (Pin 10) and to the negative logic NAND gate U16B. When the transmitter last bit time signal X BIT LAST is true (LOW), the output of U16B (Pin 6) is HIGH and presets flip-flop U4A at the next R N1 CLK time. This causes output Q (Pin 5) on U4A to go high and 0 (Pin 6) to go LOW, which presets the latch U21B, and enables (Pin 11) of the NAND gate U6C. The other inputs to U6C (Pin 9 and 10) are set HIGH by Q (Pin 6) of U21A. The output (Pin 8) of U6C is LOW forcing the receiver bit counter to resynchronize. One bit time later, when R N1 CLK clocks the flip-flop U4A, the X BIT LAST signal is false (HIGH) causing the D input (Pin 2) to be LOW: the flip-flop resets removing the preset signal from (Pin 10) of U21B. The same clock pulse presets flip-flop U5B making its output Q (Pin 9) HIGH; but the output of U6C (Pin 8) remains LOW forcing the receiver to be at LAST BIT time. At the next R N1 CLK flip-flop U4A will remain reset because D input is still LOW; also flip-flop U5B remains preset because both inputs J and K are LOW, so it does not change. But flip-flop U21A is preset and its output Q (Pin 6) goes LOW, which resets the data latch U21B and removes the signal FORCE RCVR LAST BIT. This allows the receiver bit counter to start counting from this bit time (which is two bit times behind the transmitter last bit) and hence the system must be unsynchronized. When the transmitter last bit signal X BIT LAST again becomes true (LOW), the flip-flop U4A is preset for one bit time, but the signal to resynchronize the receiver- FORCE RECEIVER LAST BIT - is not sent because the flip-flop U21A is held preset, and Q (Pin 6) is (LOW).

(b) When the normal mode is again selected, input K (Pin 10) of flip-flop U5B is set HIGH by the control flip-flop U7A (RCVR 3). Upon the next R N1 CLK signal flip-flop U5B is reset, followed one clock time later by the resetting of flip-flop U21A, which removes the reset signal from the data latch, U21B.

(5) RCVR 7 UN -SYNC B. - The purpose of this block is to prevent an ARQ CYCLE lock-up in the test mode. It consists of two flip-flops U14A and U14B (Figure A-16). Referring to logic diagram A -49 the flip-flop U14A is clocked by receiver timing signal R L N2 CLK, which occurs at the beginning of the receiver last bit time. Flip-flop U14B is clocked by receiver timing signal R L N1 CLK, which occurs at the end of the receiver last bit time. The transmitter clears the ARQ flag with the signal X CL ARQ FLG, which is active (LOW) for two character times. This signal is the D input (Pin 2) of flip-flop U14A, which is clocked by R L N2 CLK at the beginning of last bit time. It is-shifted into flip-flop U14B by R L N1 CLK at the end of last bit time. This generates the anti lock-up signal TEST UN SYNC.

(6) RCVR 8 ARQ Counter Skip On Re-Sync. - The purpose of this block is to generate a timing signal called R ARQ CT SKP, which goes false (HIGH) after four bit times in 8-bit constant ratio code format and after five bit times in II- bit constant ratio code format. It is used to determine if a re-synchronizing command is early or late. If the resynchronization occurs while R ARQ CT SKP is true (LOW), the ARQ counter skips the character count. The ARQ counter skip On Re-Sync consists of logic gates U3B (Figure A-1) U6B (Figure A-6), U10C (Figure A-6), U11C (Figure A-2) U11D (Figure A-2), U12D (Figure A-1), U12E (Figure A-1) U22C (Figure A-3) and U22D (Figure A-3). In the 8-bit constant ratio code format U10C has control signal CODE 11 BIT applied to input (Pin 10), which forces the output of U10C (Pin 8) HIGH enabling NAND gate U11D. Also U6B input (Pin 3) is held HIGH by the control signal CODE 8 BIT. The other two inputs are connected to the third and fourth bits of the receiver bit counter via inverters U12E and U12D; hence they remain HIGH until the receiver bit counter equals a count of four, after which one or both are LOW causing a HIGH at the output of U6B (Pin 6). As a result the output of U11D (Pin 11), goes LOW, and makes the output signal generated via U3B go HIGH. Hence, after receiver bit 4 the signal R ARQ CT SKP goes false (HIGH). In the 11-bit constant ratio code format the roles of U6B and U10C are reversed; input (Pin 11) on U10C is connected to the fourth bit of the receiver bit counter via the inverter U12D; but the second input (Pin 9) on U10C is connected to BIT 4 (BIT 1 + BIT 2), which is LOW on the fifth count and remains LOW for the remainder of character time. Thus, after receiver bit 5 the signal R ARQ CT SKP goes false (HIGH).

(7) RCVR 9 Clock Step Generator. - The purpose of this block is to generate the receiver output step clock timing signal R CLK ST. In start-s top modes this is a negative-going pulse for one bit time with the trailing edge making the first data bit (ie. the start-bit); but in bit stream it is six periods of the R CLK timing signal gated so that the first cycle of the step clock signal R CLK ST occurs at the same time as the first data bit. Thus, the fall of R CLK ST or the rise of R CLK ST occurs at the center of each bit stream data bit. The clock step generator consists of two flip-flop U5A (Figure A-15) and U4B (Figure A-14); three NAND gates U10B, U6A (Figure A-6), and U9B (Figure A-6); four inverters U12F, U3A, U3C (Figure A-1) and U2B (Figure A-2); and NOR gate U11A (Figure A-2).

(a) In start-stop modes flip-flop U4B is reset by the initialization signal INIT 1-1 and clocked at the rise of the timing signal R CLK 1. The D input (Pin 12) of U4B is connected to the timing signal R BIT LAST; its output Q (Pin 9) goes HIGH at the first rise of the receiver clock R CLK 1 after the timing signal R BIT LAST becomes true (HIGH). This step clock signal, which occurs once per character after last bit time, is gated by NAND gate U6A: first for the selected mode (control signal BIT STREAM is false (HIGH) at input Pin 13); and second for an output character to the data sink

(Not a mutilated or supervisory character determined by the control signal R OUT EN at input Pin 2). The enabled step clock signal is logically OR'ed with that generated for the bit stream mode by the negative logic NOR gate U11A and buffered by inverter U2B to generate the output step clock signal R CLK ST (This is again inverted into the system output signal R CLK ST L by the line driver (RCVR 29) on circuit card A2A8.

(b) In bit stream mode flip-flop U5A is reset by the initialization signal INIT 1-1 and clocked at the fall of the timing signal R N2 CLK. Input terminal J (Pin 14) of U5A is connected to the timing signal R BIT LAST; its output Q (Pin 2) goes HIGH at the first fall of R N 2 CLK after R BIT LAST becomes true (HIGH). The K input (Pin 3) of U5A goes HIGH after a count of six receiver bit times (decoded from the receiver bit counter, RCVR 5 by **U12F, U10B,** and U3A). Its output Q (Pin 12) goes LOW at the first fall of R N2 CLK after six bit times have been counted. This step clock signal, which is HIGH for six bit times per character, is gated by NAND gate U9B: first for the selected mode (Control Signal BIT STREAM true (HIGH) generated from BIT STREAM by U3C); second for an output character to data sink (determined by the control signal R OUT EN); third by the receiver clock signal R CLK 1. The output of U9B (Pin 8) is six complete periods of the receiver clock signal R CLK 1. It is logically OR'ed with the start stop version of the step clock by the NOR gate **U11A,** buffered by inverter U2B to produce the output signal R CLK ST. This signal can be monitored at test point TP1. Refer to the timing diagram (Figure A-65) for the complete timing and wave shape of this signal in the two modes of operation.

(8) RCVR **10** Data Inhibit Control. - The purpose of this block is to inhibit data characters being sent to the data sink terminal; if the system is in an ARQ or SYNC cycle; or if a supervisory control character has been received. The data inhibit control block consists of two flip-flop **U13A** and U13B (Figure A-16), two NOR gates U20 (Figure A-8) and U22B (Figure A-3), and two inverters U12C (Figure **A-1)** and U22A (Figure A-3). Both flip-flops are reset by the initialization signal INIT 1-1 and are clocked by the receiver timing signal R L N2 CLK, which occurs at R N2 CLK time only during last bit time. The supervisory character signal **IDLE RCVD** is applied to the D input (Pin 12) of flip-flop **U13B,** and if true (LOW) at the receiver last bit time its output Q (Pin 9) becomes active LOW, generating the signal R IDL INH. This causes an all 1's character to be sent to data sink (IDLE) but does not inhibit the clock step generator. The supervisory character signals **ARQ RCVD, INH ACT RCVD, INH DEACT** RCVD, SYNC A RCVD, and **SYNC B RCVD**- -together with the control signal R SYNCING--are logically OR'ed by the negative NOR gate U20, which generates the control signal **SUPER RCVD** at its output (Pin 8) and test point TP8. This signal is inverted by gate U12C and becomes the output signal SUPER RCVD. The control signal R IN ARQ is inverted by U22A, then OR'ed to the signal SUPER RCVD by U22B. Thus the output of NOR gate U22B (Pin 4) is LOW if any supervisory

character (except IDLE) is received, or if the receiver is in ARQ or SYNC cycle. This output is connected to the D input (Pin 2) of flip-flop U13A; if active (LOW) at the receiver last bit time, it causes the signal R OUT EN to be false (LOW), which inhibits the data to the data sink terminal (sends all HIGH's), and inhibits the receiver step clock signal R CLK ST.

(9) RCVR 11 Data Timing. - The purpose of this block is to retime the data leaving the parallel-to-serial converter so that the data sent to the data sink terminal is in phase with the receiver clock signal R CLK - and changes at its rise time. The block consists of a single flip-flop U19A (Figure A-14) which is clocked by the receiver clock signal R CLK 1. The output data signal from the parallel-to-serial counter (RCVR 18) on board assembly A2A9 is applied to the D input (Pin 2) of U19A. The data output signal R O DA B taken from the Q output (Pin 6) of U19A is therefore a retimed data signal with equal bit times and phased with the receiver clock signal R CLK 1. This signal is inverted in the line driver (A2A8) and becomes the output signal to the data sink. The wave shapes of these signals are illustrated in the timing diagrams of Figures A-65 and A-66.

d. A2A11 RCVR ARQ and SYNC Control (Logic Diagram Figure A-50, Block Diagram Figure A-39, Wiring Diagram Figure A-77, Timing Diagram Figures A-66 and A-68).

(1) RCVR 20 Mutilated Character Indicator. - The purpose of this block is to generate signals to indicate when a mutilated character (Non-constant ratio code, or unused) has been received; these signals MC IND and MC IND FP are used for the remote location and front panel respectively. The mutilated character indicator consists of the flip-flop U20A (Figure A-15) NAND gate U14B (Figure A-2), NOR gate U14A (Figure A-2) and two inverters U6C and U16B (Figure A-1). Referring to the logic diagram (Figure A-SO) the two control signals NCR RCVD and UN-USED RCVD are logically OR'ed by the negative logic NOR gate U14A. The output of this gate (Pin 3) is enabled at the receiver last bit time by the NAND gate U14B. Thus the output of U14B (Pin 6) is LOW if the control signals NCR RCVD or UN-USED RCVD are true (LOW) at the receiver last bit time. This signal is inverted\ by U6C and becomes the J input (Pin 14) of the J-K flip-flop U20A. The K input (Pin 3) is connected to the ARQ control signal ARQ CYCLE, which is true (LOW) when the receiver is in an ARQ cycle, hence it is normally HIGH. The flip-flop U20A is reset by the initialization signal INIT 1-1 at power turn-on and is clocked by the receiver clock signal R CLK. Hence if an unused or non-constant ratio code is received, the flip-flop U20A toggles at the fall of R CLK, which makes output Q (Pin 12) HIGH, and drives the front panel LED via the driver U16B and resistor R3 (330 Ohms). The Q output (Pin 13) is driven LOW producing the indicator signal MC IND for remote indication via line driver (A2A8); it also resets flip-flop U24B in RCVR 22.

(2) RCVR 21 Synchronizing Pattern Detector. - The purpose of this block is to determine if the receiver has received the synchronization pattern consisting of supervisory character SYNC A followed by SYNC B. This pattern consists of eight consecutive 1's followed by four or seven 0's depending upon code format. The block consists of 4-bit counter U8 (Figure A-18); a flip-flop U13B (Figure A-15); two NAND gates U14D (Figure A-2), U15C (Figure A-4); three NOR gates U7B, U7C (Figure A-3), U14C (Figure A-2); and four inverters U6A, U6D, U16A (Figure A-1), U23C (Figure A-2).

(a) Referring to the logic diagram (Figure A-50) flip-flop U13B is reset by the initialization signal INIT 1-1; counter U8 is reset to zero count by the initialization signal INIT 1-1 (generated from INIT 1-1 by U6B) via the NOR gate U7B. The counter is also reset to zero by the next clock pulse R N1 CLK when the count reaches 15 and the maximum count output (Pin 15) goes HIGH. The reset is accomplished through U7B. This signal can be monitored at the test point TP1. The counter is clocked at every bit time by the timing signal R N1 CLK; but below a count of four (QC and QD LOW) it is disabled by NOR gate U7C and U14C setting the counter enable (Pin 7) LOW.

(b) When the signal SYNC A RCVD becomes true (LOW), four l's have been detected on the data lines R CODE 10, R CODE 9, R CODE 8, and R CODE 7. These might be the four consecutive 1's of the supervisory character SYNC A. The signal SYNC A RCVD sets the J input (Pin 7) of flip-flop U13B HIGH, through inverter U6D, and enables NAND gate U14D to generate a load signal (Pin 11) and to enable the counter via NOR gate U14C. The next clock signal R N1 CLK presets flip-flop U13B through inverter U16A, which disables NAND gate U14D. Disabling U14D accomplishes two things:

1. It loads counter U8 with the contents of data inputs A, B, C, D,
2. It prevents counter 8 from being reloaded.

Data inputs A,B,C,D depend upon the constant ratio code in use. They are determined by the control signals CODE 8 BIT and CODE 11 BIT and are set -- for a count of eight or five in 8-bit or 11-bit constant ratio code, respectively. Counter U8 is now enabled to count and is incremented every bit time by clock signal R N1 CLK.

(c) Consider now the system working in the 8-bit constant ratio code. When SYNC A RCVD goes TRUE (LOW), counter U8 is loaded with a count of 8 and the data lines R CODE 7 through R CODE 10 are all 1's (Also data line R CODE 6 must be 0). At each bit time the clock signal R N1 CLK shifts the data on the data lines towards lower numbers (ie. 1→2 or 3→2) and increments the counter, U8. After eight bit times the counter reaches maximum count (15) and the carry output (Pin 15) is HIGH. Also, one complete constant ratio code (8 BITS) has been shifted along the data lines. If a

real synchronization pattern is being received, the second supervisory synchronization character SYNC B is on the data lines R CODE 3 through R CODE 10. (Data lines R CODE 3 through R CODE 6 are all HIGH; and R CODE 7 through R CODE 10 are LOW.) The signal SYNC B RCVD is true (LOW) when the data lines R CODE 3 through R CODE 6 are all HIGH, and the signal SYNC 0 RCVD is true (LOW) when the data lines R CODE 7 through R CODE 9 are all LOW. Thus when the second supervisory synchronization character-SYNC B - is received, the signals SYNC B RCVD and SYNC 0 RCVD are both true (LOW). After 8 counts of counter U8, when Carry Out is HIGH, the NAND gate U15C examines the signals SYNC B RCVD (generated from SYNC B RCVD by U6A) and SYNC 0 RCVD (generated from SYNC 0 RCVD by U23C). If both are true at this bit time, the output of U15C (Pin 8) goes LOW generating the signal R RE-SYNC. This forces the receiver to resynchronize on this character. Counter U8 is then reset and disabled from counting by the next clock signal R N1 CLK. It remains so until the signal SYNC A RCVD is again true. The enable flip-flop U13B, which was preset when SYNC A RCVD went true (LOW), is reset when the four l's that generated the signal SYNC A RCVD reach the SYNC B detector and generate the signal SYNC B RCVD five bit times later. The signal SYNC B RCVD is inverted by U6 and becomes the K input (Pin 10) for U13B, resetting the flip-flop at the clock signal R N 1 CLK. If the incoming data pattern has eight consecutive 1's (correct sync pattern) the inputs J and K of U13B are both HIGH for one data bit time. The flip-flop toggles (Resets). But if nine consecutive data l's are received, the inputs J and K are both HIGH for two data bit times and the flip-flop toggles twice, forcing a new load on counter U8 and starting a new search sequence.

(d) In the 11-bit constant ratio code counter U8 is loaded with a count of 5 and hence must count 11 data bit times before maximum count occurs. The timing sequence in this mode follows the same logical pattern as that described above in paragraph (c) for the 8-bit constant ratio code. A true resynchronization pattern has been received when the output of this block signal R RESYNC goes true LOW for one character time. (This signal can be monitored at test point TP2.) It forces this bit time to become the receiver last bit time, generating the timing signal R LAST BIT (RCVR 5).

(3) RCVR 22 TWO ARQ's Detector. - The purpose of this block is to detect two sequential ARQ supervisory characters that must be received during an ARQ cycle to enable the receiver to leave the ARQ mode. The detector consists of: flip-flop U24A (Figure A-16); three NAND gates U25A. U25B (Figure A-3) and U23A (Figure A-2); a NOR gate U25C (Figure A-3); an inverter UPOF (Figure A-1); and a data latch U24B (Figure A-14).

(a) Data latch U24B is initially preset by the initialization signal INIT 1-1 applied to input (Pin 8) of the NOR gate U25C; it is reset by the indicator signal MC IND applied at reset input Pin 13 when a mutilated character is detected.

(b) When the receiver enters the ARQ cycle, the control signal ARQ CYCLE goes true (LOW) and enables the NAND gate U25A on (Pin 2). If an ARQ supervisory character is received, the signal ARQ RCVD also goes true (LOW) making the output of U25A HIGH--which is the D input (Pin 2) of flip-flop U24A. The flip -flop is clocked at Last bit time by the clock signal R L N1 CLK. If an ARQ supervisory character is on the data lines, and the receiver is in an ARQ CYCLE, the flip-flop is preset causing Q (Pin 6) to go LOW. This enables NAND gate U25B. The other input to this gate is the supervisory character ARQ RCVD at Pin 5. If the next character is also an ARQ supervisor, the output of U25B (Pin 4) goes HIGH, This is examined at the last bit time by NAND gate U23A; if true, it presets data latch U24B via inverter U10F and NOR gate U25C. The data latch generates the output signal TWO ARQ's RCVD. If the next character is not an ARQ supervisor, flip-flop U24A is reset, and the sequence is repeated.-

(4) RCVR 23 Initialize ARQ and SYNC Counters. - This block generates the load signals required to initialize the ARQ and SYNC character counters. It consists of four NOR gates U4A, U4B, U4C, and U4D (Figure A-2). The memory length select signals MEM LG 4, MEM LG 8, MEM LG 16, and MEM LG 32 are logically OR'ed to the initialization signal INIT 1-1 so that, at initialization time, the outputs of the negative logic NOR gates U4A, U4B, U4C and U4D are all HIGH- -and independant of the memory length switch setting. These outputs generate the signals that load the ARQ and SYNC character counters when a load enable is applied. The counters have asynchronous loads and therefore do not require a clock pulse.

(5) RCVR 24 ARQ Cycle Counter. - The purpose of this counter is to count the number of characters that the receiver blanks out from the data sink during an ARQ cycle. The counter consists of a 4-bit counter U3 (Figure A-19); two J-K flip-flops U21A, U21B (Figure A-15); six NAND gates U7A (Figure A-3) U9B, U17C, U17D (Figure A-2) U11A, U15A (Figure A-6); two NOR gates U5A, U9C (Figure A-2); and six inverters U10A, U10C, U10D, U10E, U19E, U19F (Figure A-1).

(a) The counter U3 is loaded with maximum count (15) and the two flip-flops U21A and U21B are reset by the initialization signal INIT 1-1 applied to load input (Pin 11) of counter U3 via NOR gate U5A and inverter U19E This provides a direct load of counter U3 and a reset signal to flip-flop U21A and U21B. After four counts the Q outputs of these flip-flops are both HIGH, which enables the NAND gate U17C to enable NAND gates U17D and U15A via inverter U10A. NAND gate U17D is also enabled by the carry signal (Pin 12) of counter U3. The counter is set to maximum count. U17D output (Pin 11) is LOW preventing J-K flip-flop U21B from counting and disabling counter U3 via NAND gate U15A. The output of NAND gate U17D also sets the K input (Pin 3) of flip-flop U18A LOW, and--via the inverter U10D--the J input (Pin 14) is set HIGH so that the next timing signal R L N2 CLK presets flip-flop U18A. This

enables NAND gate U11A. This is the normal state for the ARQ counter when the receiver is processing normal data characters. The control signal ARQ CYCLE is false (HIGH) when the counter is in the normal state. lt can be monitored at test point TP4.

(b) The receiver initiates an ARQ cycle when the control signal ST ARQ is set HIGH by the ARQ flag logic (RCVR 26). This signal is inverted by inverter U10C and logically OR'ed by negative logic NOR gate U9C to the counter maximum count signal ARQ CYCLE, which with normal data flow is always HIGH. This generates the signal R IN ARQ and--via the inverter U19F--the output control signal R IN ARQ, which is true (LOW) for the duration of the ARQ sequence; it disables the receiver output to the data sink and halts the receiver step clock signal. The control signal R IN ARQ disables the inhibit supervisory character flag logic (RCVR 27) and enables NAND gate U11A so that the next timing signal R L N1 CLK presets the ARQ FLAG flip-flop U20B (Part of ARQ flag logic (RCVR 26)). This forces counter U3 to load the contents of the A, B, C, and D inputs by setting the load input (Pin 11) LOW via negative logic NOR gate U5A and inverter U19E. This LOW signal also resets counter flip-flops U21A and U21B. The actual count loaded into counter U3 by the load signal depends upon the length selected for the transmitter memory, and coded in the memory length control signals MEM LG 4, MEM LG 8, MEM LG 16 and MEM LG 32. The truth table showing the relationship between memory length selected and the state of the four control signals is shown in Table 4-13. The memory length control signals are combined with the initialization signal INIT 1-1 and inverted by the counter initialization logic (RCVR 23) so that the signals that are loaded into counter U3 are the complements MEM LG 4, MEM LG 8, MEM LG 16 and MEM LG 22 of those shown in the Table 4-13. These signals are connected to the data inputs A, B, C and 17, of counter U3 and are directly loaded into the counter when the load terminal (Pin 11) goes LOW.

(c) The ARQ counter, when enabled, is incremented once per character by the timing signal R L N2 CLK, which occurs at the beginning of the receiver last bit time; it is generated from the signal R L N2 CLK by inverter U16F. This ARQ counter clock signal is gated by NAND gate U9B, which prevents the counter from counting when the control signal R ARQ CT SKP is true (LOW). Inverter U10E, via NAND gate U15A, enables counter U3 (Pin 4) when clock signal R' L N2 CLK 1 is LOW. At the same time, it clocks the two J-K flip-flops U21B and U21A (the two flip-flops change state on the fall of the clock). The signals R ARQ CT SKP and R L N1 CLK can be monitored at the test points TP7 and TP8 respectively.

(d) The receiver always enters the ARQ cycle at the beginning of the receiver last bit time when the control signal ARQ CT SKP is false (HIGH). Refer to the receiver timing diagrams Figures A-65 and A-66. Hence the ARQ counter clock signal R L N2 CLK 1 is enabled by NAND gate U9B.

TABLE 4-13. Memory Switch Truth Table

MEMORY LENGTH	SWITCH SETTING	MEM LG 4	MEM LG 8	MEM LG 16	MEM LG 32
4	0	0	0	0	0
8	1	1	0	0	0
12	2	0	1	0	0
16	3	1	1	0	0
20	4	0	0	1	0
24	5	1	0	1	0
28	6	0	1	1	0
32	7	1	1	1	0
36	8	0	0	0	1
40	9	1	0	0	1
44	10	0	1	0	1
48	11	1	1	0	1
52	12	0	0	1	1
56	13	1	0	1	1
60	14	0	1	1	1
64	15	1	1	1	1

During a resynchronization sequence (SYNC CYCLE) the timing of the receiver last bit time, and therefore the timing signal R L N2 CLK, is changed to resynchronize the receiver to the distant transmitter. If the new timing for the receiver last bit occurs during the first half of a character, it is assumed to be caused by a &lay in the propagation time; the control signal ARQ CT SKP--which depends upon the receiver bit count before resynchronization--is true (LOW), and the new last bit time is not counted. This prevents the same character being counted twice. But if the new timing for the receiver last bit time occurs during the last half of a character, it is assumed to be caused by an advancement in the propagation time and the control signal ARQ CT SKP is false (HIGH), which enables the character that arrived early to be counted. The ARQ counter is able to keep count of the number of characters transmitted provided the system synchronization does not change by more than ± half a character time. The timing for the ARQ CT SKP signal in the two constant ratio code lengths is illustrated in the timing diagrams (Figures A-65 and A-66).

(e) After being loaded, the ARQ counter is not at maximum count. The ARQ control signal ARQ CYCLE becomes true (HIGH) enabling J-K flip-flop U21B to count and one character later the timing signal R L N2 CLK resets flip-flop U18A, which disables NAND gate U11A preventing the ARQ flag being reset or the ARQ counter being reloaded. The signal ARQ CYCLE generated by inverter U10D from the signal ARQ CYCLE holds the signal R IN ARQ active (HIGH) via the negative logic NOR gate U9C and enables flip-flop U21A to count via the negative logic NAND gate U7A. The timing signal R L N2 CLK also toggles the flip-flop U21B (through NAND gate U9B and inverter U10E, which enables U21A via the negative logic NAND gate U7A; so that at the next occurrence of the timing signal R L N2 CLK (another character later) the flip-flop U21B is reset and flip-flop U21A is set. Flip-flop U21B and U21A from a synchronous 2-bit counter; after four characters the Q outputs (Pin 9 and 12) of both flip-flops are HIGH. This enables NAND gate U17C, which enables NAND gates U17D and U15A through inverter U10A. NAND gate U17D checks counter U3 for maximum count and, if true, its output goes LOW. This sets the signal ARQ CYCLE false (LOW). The next timing signal R L N2 CLK--occuring at the beginning of the receiver last bit time--presets flip-flop U18A. NAND gate U11A is enabled, so that if the ARQ flag logic (RCVR 26) has initiated another ARQ sequence on the last character of the old one, counter U3 is reloaded and the ARQ flag flip-flop U20B is preset by the timing signal R L N1 CLK, which occurs at the end of the receiver last bit time, If the last character of the ARQ cycle is correctly received, the receiver leaves the ARQ cycle. If counter U3 is not at maximum count when a count of four characters is reached, NAND gate U15A is enabled, which enables counter U3 to increment one count at the next timing signal R L N2 CLK 1. This also resets both flip-flops U21B and U21A and the sequence repeats, with every fourth character incrementing counter U3 until maximum count is reached. Changing the number loaded into counter

U3 between 15 and 0 changes the number of characters counted for the ARQ cycle between 4 and 64, with increments of four characters. The ARQ character count is dependent upon the memory length control signals MEM LG 4, MEM LG 8, MEM LG 16 and MEM LG 32.

(6) RCVR 25 SYNC Cycle Counter. - The purpose of this counter is to count two complete memory lengths menus two characters, which is the number of characters in the system sync cycle. The two synchronizing supervisory characters SYNC A and SYNC B are not counted; hence the complete synchronization cycle is two complete memory lengths. The sync cycle counter consists of two 4-bit binary counters U1 and U2 (Figure A-19; a J-K flip-flop U18B (Figure A-15); three NAND gates U11B (Figure A-4). U9A and U9D (Figure A-2); three NOR gates U11C (Figure A-6), U17A and U17B (Figure A-2); and six inverters U19B, U19C, U19D, U16C, U10D, and U18F (Figure A-1).

(a) At initialization time both the counters U1 and U2 are loaded with maximum count by the initialization signal INIT 1-1 applied to the input (Pin 5) of the negative logic NOR gate U17B and inverted by U16C to generate the load signal (Pin 11) on the counters U1 and U2. (This is an asynchronous load and hence requires no clock pulse). The carry outputs of both counters (Pin 12) are HIGH; therefore both inputs of the NAND gate U9A are HIGH, and its output (Pin 3) is LOW. This is inverted by U16F to generate the signal R SYNC MAX CT, which disables the counter U1 (Pin 4) and causes the sync cycle enable flip-flop U18B to be reset when clocked by the RL N1 CLK signal. Also, the output of the NAND gate U9D (Pin 11) is HIGH (input is set LOW by the carry signal of U2 inverted by U19B); this disables the counter U2. This is the normal condition of the sync counter when the system is not processing a sync cycle.

(b) The sync cycle is initiated when the sync pattern detector (RCVR 21) detects the supervisory characters SYNC A followed by SYNC B and generates the control signal R RE SYNC. This is applied to the negative NOR gate U11C (Pin 9). Output of U11C is the signal R SYNCING, which is inverted by U19D to produce the output signal R SYNCING. The control signal R SYNCING is also applied to the NAND gate U11B (Pin 5) which is enabled by the sync cycle enable flip-flop U18B (output Q Pin 8 HIGH). The sync signal R RE SYNC forces the present bit time to be LAST BIT time; hence the timing signal R L N2 CLK occurs at the beginning of the present bit time and the output of the NAND gate U11B (Pin 6) goes LOW. The negative logic NOR gate U17B and the inverter U16C generates a load signal to the counters U1 and U2 (Pin 11).

(c) The actual count loaded depends upon the memory length selected and coded in the control signals MEM LG 4, MEM LG 8, MEM LG 16, and MEM LG 32 (See Table 4-13 for the truth table). The coded signals are log-

ically OR'ed with the initialization signal INIT 1-1 and inverted by the counter initialization block (RCVR 23), and becomes MEM LG4 + INIT 1-1, MEM LG 8 INIT 1-1, MEM LG 16 + INIT 1-1 and MEM LG 32 + INIT 1-1 These load the counters U1 and U2. For example, if memory length is 20 characters, then MEM LG 4 = 0, MEM LG 8 = 0, MEN LG 16 = 1 and MEM LG 32 = 0, The counter U1 is loaded with a count of 9 and counter U2 with a count of 13. The carry outputs (Pin 12) on both counters go LOW making the output of NAND gate U9A (Pin 3) HIGH; this enables counter U1. (Pin 4) via inverter U16F and causes the sync control signal R SYNC MAX CT to go LOW, which holds the R SYNCING signal active via negative logic NOR gate U11C (Pin 10). The sync cycle enable flip-flop U18B is preset at the beginning Of the next last bit time; its output Q (Pin 8) goes LOW disabling NAND gate U11B and holding the R SYNCING signal true via (Pin 11) of the NOR gate U11C. The counter U1 is incremented once per character at last bit time by the timing signal R L N2 CLK. After 6 characters the counter reaches maximum count (15) and the carry output (Pin 12) goes HIGH. This enables NAND gate U9D and its output (Pin 11) goes LOW; this enables the counter U2. At the next clock Pulse R L N2 CLK the counter U2 is incremented to a count of 14, and counter U1 is reset. Counter U1 is now incremented for each character, and after 15 characters is again at maximum count. Counter U2 is then enabled and on the 22nd character (6 + 16) the counter U2 is again incremented, this time to maximum count 15 when the U1 counter is reset. The U1 counter is again incremented every character until maximum count is reached, when a carry output (Pin 12) is generated; this enables NAND gate U9A because counter U2 is also at maximum count. Hence the output of U9A is LOW, the sync control signal R SYNC MAX CT HIGH via U16F, disabling the counter U1 (Pin 4). The sync enable flip-flop U18B is reset at the beginning of the next last bit time. The output signal R SYNCING remains TRUE (LOW) from the fall of the resync signal R RE SYNC until the sync enable flip-flop U18B is reset--two complete memory cycles.

(7) RCVR 26 ARQ Flag. - The purpose of this block is to generate the signal ST ARQ that initiates a receiver ARQ sequence, and the signal R ARQ FLG that informs the transmitter that the receiver has detected a mutilated character or received the supervisory character ARQ. The block consists of a J-K flip-flop U20B (Figure A-15); two NOR gates U22A, U22B (Figure A-6); and a NAND gate U15B (Figure A-6).

(a) The control signal ST ARQ is generated by the negative logic NOR gate U22B if the control signals NCR RCVD, UN USED RCVD, ARQ RCVD, or TWO ARQ RCVD are LOW at the receiver last bit time, and the ARQ counter (RCVR 24) is at maximum count (ARQ CYCLE false (HIGH)); or if the transmitter or receiver is processing a sync cycle. The control signals NCR RCVD, UN USED RCVD, ARQ RCVD, TWO ARQ'S RCVD are logically OR'ed by the negative logic NOR gate U22B and the output (Pin 8) is

enabled by NAND gate U15B when the ARQ counter is at maximum count (ARQ CYCLE false (HIGH)) and the receiver is at last bit time (R BIT LAST true (HIGH)). NAND gate U15B output (Pin 6) is logically OR'ed to the control signals X SYNCING and R SYNCING by negative logic NOR gate U22A, which generates the output signal ST ARQ. When true (HIGH) this inhibits the flow of data to the data sink, halts the receiver step clock, and initiates a receiver ARQ cycle.

(b) The ARQ flag signal R ARQ FLG is generated by flip-flop U20B, which has the control signal ST ARQ connected to its J input (Pin 7) and is clocked by the timing signal SET ARQ FLG. SET ARQ FLG occurs at $\overline{R}$ L N1 CLK time--only during the first character of a receiver ARQ cycle. Therefore, the ARQ flag signal R ARQ FLG can be set only at the first character of the receiver ARQ cycle. The flag is cleared directly by the transmitter on the first character of the transmitter ARQ cycle by the control signal X CL ARQ FLG which is connected to the reset (Pin 6) of flip-flop U20B.

(8) RCVR 27 Inhibit Flag. - The purpose of this block is to generate the signal INH ACT FLG, which informs the transmitter that the inhibit activate supervisory character has been received, The inhibit flag logic consists of: the flip-flop U13A (Figure A-15); NOR gate U7D (Figure A-3); NAND gate U5D (Figure A-2); and inverters U5C (Figure A-2), U6E and U6F (Figure A-1).

(a) The supervisory signal INH ACT RCVD is inverted by U6E and constitutes the J input of flip-flop U13A; the supervisory signal INH DEACT KCVD inverted by U6F forms the K input of U13A. The flip-flop is clocked at the beginning of the receiver last bit time by the timing signal R L N2 CLK, which is disabled by NAND gate U5D if the system is in an active ARQ or SYNC cycle. The control signals R SYNCING and R IN ARQ are logically OR'ed in NOR gate U7D and disable the NAND gate U5D at input (Pin 12). The inhibit flag logic is therefore inactive during a system ARQ or SYNC cycle,

(b) The output terminal Q (Pin 12) of flip-flop U13A generates the output signal INH ACT FLG; when active (HIGH) it informs the transmitter that the last inhibit supervisory character received was Inhibit Activate. The output signal goes LOW when the supervisory character Inhibit Deactivate is received. The inhibit flag signal INH ACT FLG is reset (LOW) at initialization time by the initialization signal INIT 1-1 connected to the reset terminal (Pin 2) of U13A.

(9) RCVR 28 Sync Flag. - The purpose of this block is to generate the two flag signals R SYNC FLG 1, which informs the transmitter that the sync pattern has been detected and forced the receiver to re-synchronize; and R SYNC FLG 2, which informs the transmitter that either the Inhibit Activate or the Inhibit Deactivate supervisory characters have been received correctly

by the resynchronized receiver. The sync flag logic consists of: two flip-flops U12A and U12B (Figure A-15); NOR gates U23A and U5B (Figure A-2); inverters U19A (Figure A-1) and U23B (Figure A-2). The initialization signal INIT 1-1--via NOR gate U23A and inverter U23B--reset flip-flop U12B at the direct reset input (Pin 6). This clears the sync flag signal R SYNC FLG 1 and--with the Q output (Pin 9) --resets flip-flop U12A at its direct reset input (Pin 2). Thus, both the sync flags are inactive (HIGH) after initialization. When the sync pattern detector detects the synchronizing sequence, it generates the control signal R RE SYNC, which is inverted by U19A and forms the J input (Pin 7) of U12B at the beginning of the next bit time (forced last bit time). The timing signal R L N2 CLK clocks flip-flop U12B and activates the flag signal R SYNC FLG 1 (LOW). It also removes the reset from U12A (Pin 2). The signals INH ACT RCVD and INH DEACT RCVD are logically OR'ed in negative logic NOR gate U5B; if either is true (LOW) at the new last bit time, flip-flop U12A is preset and generates the flag signal R SYNC FLG 2 at its Q output (Pin 13). Both flags are cleared (set HIGH) by the transmitter signal X CL SYNC FLGS, which is applied to the direct reset (Pin 6) of U12B via the NAND gate U23A and inverter U23B. This resets U12B, which resets U12A, clearing both flags.

CHAPTER 5

PREVENTATIVE MAINTENANCE

I - PREVENTATIVE MAINTENANCE PROCEDURE

5-1. GENERAL. - Preventative maintenance procedures described herein relate to the AN/FYC-12 operating as a system.

5-2. TOOLS AND TEST EQUIPMENT. - No special tools are required. Table 5-1 lists the test equipment required for preventative maintenance. Equivalent items may be substituted.

Table 5-1. Test Equipment Required

EQUIPMENT	PURPOSE
Multimeter, Simpson 260	Power Supply Adjustment

5-3. PREVENTATIVE MAINTENANCE SCHEDULE. - Table 5-2 lists the time schedule for preventative maintenance, the inspection or maintenance required, and the items involved.

Table 5-2. Schedule of Preventative Maintenance

ITEM	INSPECTION OR MAINTENANCE REQUIRED	TIME (Days)
Power Supplies	Power supplies within ±10% tolerance	7
Equipment surfaces and cabinet interiors	Cleanliness, corrosion, foreign matter	28
Connectors	Broken pins, foreign matter between pins, damage to external casing or threads	84
Switches	Security, damage, proper orientation, positive action	84
Component and Hardware Mounting	Check for loose or missing hardware, and tighten	84

5-4. MAINTENANCE PROCEDURES. - The procedures below are used in conjunction with the applicable entries in the Table 5-2; Schedule of Preventative Maintenance.

a. Power Supply Adjustments (Figure 5-1). - Check and adjust the power supplies for the voltage specified in Table 5-3 at the test points indicated. Adjust the power supplies under load for a ±10% tolerance.

b. Cleaning. - Perform the cleaning procedures as specified. Clean equipment surfaces and cabinet interiors, removing dust and other foreign matter, with a dry cloth or dust brush.

Table 5-3. DC -DC Converter Output Voltages

TEST POINT	VOLTAGE	TOLERANCE	REMARKS
TP1	+5V DC	±5%	Adjustable
TP2	+12V DC	±15%	Non-Adjustable
TP3	-12V DC	±15%	Non-Adjustable
TP4	Ground	---	---

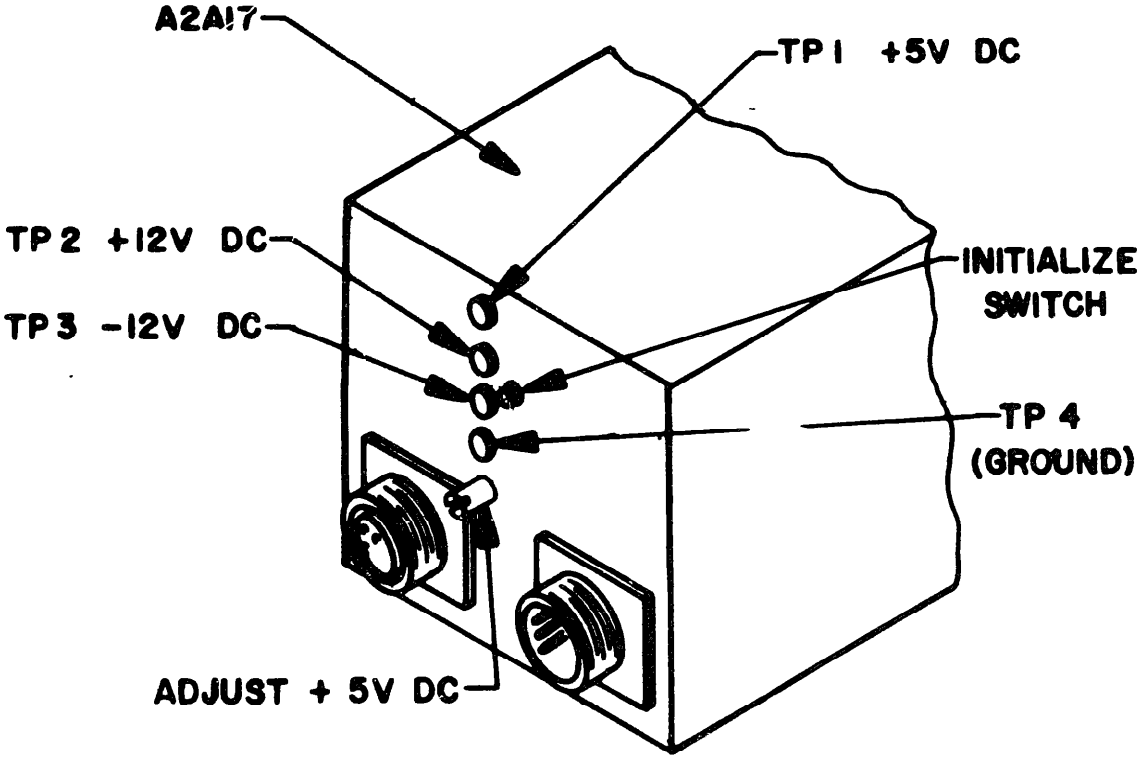

Figure 5-1. DC -DC Converter Test Points

II - OPERATIONAL TESTS AND OPTIMUM PERFORMANCE

5-5. OPERATIONAL TESTS. - Check that all pre-adjustments (Chapter 2, Section III) have been made to both ends of communication link using Digital Data Set AN/FYC -12.

a. Readying. - Turn on power at local AN/FYC-12 and place TEST switch in ON (test). The POWER ON, TEST, MUT CHAR, ARQ, and PARITY FAIL indicators should be illuminated. Press PARITY FAIL (parity reset) switch (S4), and PARITY FAIL indicator extinguishes. Press SYNC (Initiate) switch (S3) and MUT CHAR indicator extinguishes while SYNC indicator lights for period of time dependent upon data rate and length of memory cycle in use. SYNC indicator then extinguishes, followed by ARQ indicator, leaving only the TEST and POWER ON indicators illuminated. The local AN/FYC-12 is now ready to send and receive communications. Check that distant AN/FYC-12 has been tested and placed on-line by switching TEST switch (S3) to OFF. Then place the local AN/FYC-12 on-line (TEST switch S3 is OFF).

b. Synchronizing. - The MUT CHAR and ARQ indicators light indicating that the system is not synchronized. Press the local SYNC (Initiate) switch (S3) to cause the distant receiver to synchronize with local transmitter and the local receiver to synchronize with the distant transmitter. This is indicated by the MUT CHAR indicator being extinguished and SYNC indicator lighted for two memory cycles. The SYNC indicator then extinguishes, followed by ARQ indicator. The AN/FYC-12 communication system is now synchronized.

c. Inhibit Test. - Operator should test operation of ACTIVATE/DEACTIVATE (Inhibit switch, S5). Request that the distant end send Inhibit Activate (S5 ACTIVATE position) and check that INHIBIT RCVD indicator is illuminated (if strap option “A” has been selected, local data terminal closes down). This inhibit test may be repeated in reverse direction, local AN/FYC-12 inhibiting distant station.

d. Completing Operational Testing. - To complete operational testing, "test messages" of known content and length should be transmitted in both directions. The operator should observe indicator lights. The MUT CHAR indicator may turn on, followed by the ARQ indicator, which should clear the error and extinguish the MUT CHAR indicator. Check that received message was correct with no extra characters or deletions. Complete any other performance tests dictated by the station directive, The Digital Data Set AN/FYC-12 Communication Error Detector and Correction System is now operational.

CHAPTER 6

CORRECTIVE MAINTENANCE

I - GENERAL

6-1. CORRECTIVE MAINTENANCE. - Corrective maintenance consists of repair or replacement of damaged or unserviceable components necessary to return the equipment to operational status.

6-2. RECOMMENDED TEST EQUIPMENT. - Table 6-1 lists the equipment recommended for maintenance of the AN/FYC-12 equipment, Equivalent items may be substituted.

Table 6-1. Test Equipment Required for Maintenance

Extender Card Assy (0N19964D)
Oscilloscope, Tektronix 531
Preamplifier, Tektronix Type B
Multimeter, Simpson 260
Integrated Circuit Test Clip (14 and 16 pin)

6-3. PROCEDURES. - Corrective maintenance procedures are described in the following paragraphs:

a. Circuit Card Assembly Substitutions. - All logic assemblies, including the dc-dc converter, are replaceable plug-in components. They are listed in Table 1-2. If logical or power supply problems are suspected, assembly substitution may be used to expedite the return of equipment to operational status The faulty assembly may be repaired or replaced at a later time.

Note: - The dc-dc converter (assembly A2A17) is considered not repairable.

Figure 1-3 shows the replaceable modules of AN/FYC-12. Loosen the captive screws and open front panel, and using the card extractor provided, remove suspected faulty circuit card and replace with spare assembly of the same type. It is important to remove power from the equipment with circuit breaker (S1) before removing or replacing modules.

b. Circuit Tracing. - The following types of equipment drawings are supplied in the manual to support corrective maintenance procedures: circuit card logic and block diagrams, schematic diagrams, back plane wiring list, test point locations, glossary of signal names, and circuit card assembly wiring diagrams.

(1) Circuit card assembly logic diagrams. - Figures A-40 through A-50 are the eleven circuit card logic diagrams. Each of the eleven figures represents a complete printed wiring circuit board. The logic functions are defined and given block names to assist signal tracing and logical flow within a given board. Signal names are stated in the diagram margin with connector pin numbers, and destinations. Signal inputs including power supplies and clocks are at lower margin, and signal outputs at upper margin. The digital integrated circuits are identified with Figure numbers A1 through A24 which illustrate the logical function, give truth table and replacement identification numbers.

Note: - All integrated circuits used in AN/FYC-12 are installed in 14 or 16 pin sockets for easy replacement.

(2) Circuit card assembly block diagrams. - Figures A-26 through A39 are the eleven circuit card block diagrams. Each figure represents a complete printed wiring circuit card with logic functions defined by named blocks. The pins, connectors and signal names are identical to the logic diagrams.

(3) Schematic diagrams. - Figure A-51 shows front panel (A2A12) wiring and main frame interconnections including power distribution, input and output signal connections. Switch and connector pin configurations are also given to assist with main frame and front panel troubleshooting.

(4) Back plane wiring. - The back plane interconnections between the eleven circuit card assemblies is shown in Figure A -52 which is in the form of a tabulated run list between connector pins.

Note: - The back plane is “wire wrapped” with 22 swg solid wire and extreme care must be used when checking interconnections.

(5) Test point locations. - The eleven circuit card assemblies are equipped with test points, which may be monitored without removing the circuit card from the equipment. Figure A-58 illustrates the names of the signals and the circuit card assembly on which they may be observed.

Note: - When connecting oscilloscope probe to test point, use high impedance X10 probe to avoid interference due to RFI pickup

(6) Glossary of signal names. - To aid the troubleshooter, all signals used in the AN/FYC-12 are named, and a “Mnemonic” of that name is used in logical and block diagrams to identify signals. Tables 6-2 through 6-5 list in alphabetical order signals used by the transmitter, receiver, front panel and power distribution respectively.

(7) Circuit card assembly wiring diagrams. - (Figures A-67 through A -77. The wiring diagrams show the interconnections between components located on each of the printed wiring boards. The track side wiring of printed circuit card is shown in one view, the component side wiring is shown in the second view, and the component locations are shown in the third view,

c. Integrated Circuit Modules. - The individual digital integrated circuit modules used in the AN/FYC-12 are shown in Figures A-1 through A-24, which illustrate the logical function, truth table, and pin numbers for each module. The yin layouts for the 14 and 16 pin dual in-line packages are shown in A-25. The pins are numbered clockwise, looking at the track side of the cards, with pin 1 identified by an index mark. Pin 1 of the module socket is identified by a chamfer on one corner. The pins then number counter -- clockwise.

CAUTION. - Be sure the module is correctly oriented before reinserting into socket.

d. Circuit Card Assembly Repair. - The modular construction of the circuit card assemblies facilitates repair when proper tools and repair techniques are used and normal caution exercised.

(1) Tools. - Recommended tools are a vise, a pencil-type 25 to 40 watt soldering iron, small side cutters, small needlenose pliers, a desoldering tool, and a module extractor tool such as the Augat T114-1.

(2) Procedure. -

(a) For dual in-line modules simply place the module extractor tool under the module and pull. This tool minimizes the possibility of damaging the module leads.

(b) For module holders heat each pad and remove the solder with a desoldering tool. Move each module holder pin to make sure it is free. If it isn’t try removing the solder again. When all pins are free, remove the module holder.

6-4. SIGNAL ANALYSIS. - In order to assist with troubleshooting the most important signals on each unit card assembly are described, starting with the test points on the rear connector and adding other internal signals that

may help with problem analysis. The signals that are available on test points without removing the Circuit Card are illustrated in Figure A-58 (Test Point Locations) and are clearly marked on the logic diagrams. Other signals described are marked with small letters on the logic diagrams to indicate that they are minor test points. Most problems result in a constant ARQ or SYNC cycle indication, which can be caused by a fault in any part of the communication system. The test mode should be utilized to locate the problem in one end of the system or in the interconnecting medium. This chapter describes signals used in the AN/FYC-12 and how to measure them. The timing and logic diagrams, together with the block descriptions, help the troubleshooter to define the problem.

a. Circuit Card Assembly A2A1, Data Sample Generator. - This assembly has six major test points that can be monitored without removing the circuit card.

TP	1	Sample (Bit) Counter Clock	SMPL CTR CLK
TP	2	Sample (Bit) Counter Load	SMPL CTR LD
TP	3	Transmitter Serial-To -Parallel Clock	X SP CLK
TP	4	Transmitter Input Data	X IN DA
TP	5	NOT USED	---
TP	6	NOT USED	---
TP	7	Transmitter Data Sample Enable	X DA SMPL EN
TP	8	Transmitter Start Bit Detect	X ST BIT DET

(1) Test Point 1. - The signal Sample bit counter clock (SMPL CTR CLK) occurs once per transmitter bit time and is timed to be at the center of each input data bit. - The signal is normally HIGH and has 3 microsecond negative-going pulses once per bit time. Synchronize the oscilloscope on X BIT LAST and display several character times.

(2) Test Point 2. - The signal Sample Bit Counter Load (SMPL CTR LD) occurs once per character and is LOW for one bit time after a complete character has been accepted by the Sample Enable Logic. Synchronize the oscilloscope on X BIT LAST and display several character times.

(3) Test Point 3. - The signal Transmitter Serial-To-Parallel Clock (X SP CLK) occurs once per incoming data bit (including the start bit in start-stop formats) at the center of each bit time. The signal is normally HIGH and has 3 microsecond negative-going pulses once per input data bit. Two or more transmitter bit times are blocked when no new data bits are received. Synchronize the oscilloscope on X BIT LAST and display several character

times. If the system is in an ARQ or SYNC cycle, no new data, and hence no X SP CLK, is generated.

(4) Test Point 4. - The Incoming Data signal (X IN DA) is the serial data signal from the terminal source, With normal data traffic it appears as an I pattern and cannot be synchronized on the oscilloscope.

(5) Test Point 7. - The signal Transmitter Data Sample Enable (X DA SMPL EN) is LOW during the time that the transmitter is accepting a new character from the terminal source. It occurs only with normal data flow--once per character, The number of bits times it is active (LOW) depends upon the number of bits, including start bit, in the selected terminal format. Synchronize the oscilloscope on X BIT LAST and display several character times.

(6) Test Point 8. - The signal Transmitter Start Bit Detect (X ST BIT DET) is LOW for two fast clock periods (12 microseconds) when the start bit is detected. It is only enabled in start-stop data format and occurs once per character, when the system is in normal data flow. This signal disables the Reference Time Counter once per character in all start-stop modes. Synchronize the oscilloscope on X BIT LAST and display several characters.

(7) Test Point a. - The signal Transmitter Start Sample Enable (X ST SMPL EN) is HIGH at the beginning of every character. In start-stop modes it is the inverted X ST BIT DET signal and is only HIGH for 12 microseconds; but in bit stream (except during the initialization sequence) it is the SMPL WDO signal and is HIGH for the first bit time. This signal occurs once per character and in bit stream is never inhibited; but in start-stop it depends upon the start bit being detected, and hence the transmitter step clock. Synchronize the oscilloscope on X BIT LAST and display several characters.

(8) Test Point b. - The signal Transmitter Input Data Inhibit (X IN DA INH) is LOW to halt transmitter step clock signal X ST CLK L. It is LOW when the system is processing an ARQ or SYNC cycle, which normally has a duration of one memory length. It is also LOW for one character time to transmit the supervisory characters Inhibit Activate or Inhibit Deactivate, or indeterminantly LOW when the transmitter is inhibited from the distant end. The signal has a long period or is not cyclic; use oscilloscope to determine logic state HIGH or LOW.

(9) Test Point c. - The output (Pin 8) of inverter U2D is the signal that resets the Sample Enable logic. It is the X ST SMPL EN signal enabled by the X IN DA INH signal. With normal data flow it occurs once per character and is identical to the signal at test point a.

(10) Test Point d. - The output (Pin 4) of inverter U17B is the enable signal for the Reference Time Counter. It is active HIGH when the Sample Enable logic is preset, as the last data bit is accepted from the data source, until the next start bit is detected. With normal data flow this is between two and four bit times, depending upon the selected data format. The signal occurs once per character and enables the Reference Time Counter to count fast clock periods and be reset once per bit time by the signal X P CLK. Synchronize the oscilloscope on X BIT LAST and display several characters.

(11) Test Point e. - The output (Pin 6) of NAND gate U10B is the reset signal for the Reference Time Counter. In bit stream mode it is held inactive HIGH but in all start-stop modes it is active LOW during the X P CLK time, when the Reference Time Counter is enabled. It appears as two or three negative-going 6 microsecond pulses per character time. Synchronize the oscilloscope on X BIT LAST and display several characters.

b. Circuit Card Assembly A2A2, Data Bit Generator and Fast Block. - This assembly has eight major test points that can be monitored without removing the circuit card.

TP	1	Initialize	INIT 3
TP	2	Memory address maximum	MEM ADD MAX
TP	3	Initialize 2	INIT 2
TP	4	Fast clock	FAST CLK
TP	5	Transmitter bit time 6	X BIT 6
TP	6	Transmitter bit time 1	X BIT 1
TP	7	Sample window	SMPL WDO
TP	8	Transmitter bit last	X BIT LAST

(1) Test Point 1. - The signal Initialize 3 (INIT 3) is active LOW during the initialization sequence until the first memory write pulse occurs. The signal is LOW for a period of 15 bit times and then remains inactive HIGH until the system is powered down or re-initialized. The signal holds the transmitter SEND LIN L HIGH until the first character is written into the memory. Since the signal is not periodic it may be difficult to measure without a memory oscilloscope. Use a slow time base, synchronized on the signal INIT 1, and estimate the number of bits between power turn on and the rise of INIT 3.

(2) Test Point 2. - The signal Memory Address Maximum (MEM ADD MAX) is active LOW during the first four memory addresses selected after completing one complete memory cycle. The trailing edge (RISE) is used to

reset the initialization signal INIT 2 after one complete memory cycle plus four character times. The signal is continuous, can be self-synchronized on the oscilloscope, and is LOW for four character times in the memory length selected.

(3) Test Point 3. - The signal Initialize 2 (INIT 2) is active LOW during the initialization sequence until one complete memory cycle plus four character times have elapsed. This ensures that every used memory location has the Inhibit Activate supervisory character written into it. The time required depends upon the selected memory length and the data rate. The signal, like INIT 3, is not periodic, and after the initialization sequence remains permanently inactive (HIGH).

(4) Test Point 4. - The signal Fast Clock (FAST CLK) timing signal is a periodic 153.6 KHz crystal controlled square wave. The mark-space ratio for this signal is not critical but should be within 40/60 for good timing. The oscilloscope may be self synchronized.

(5) Test Point 5. - The signal Transmitter Bit Time 6 (X BIT 6) occurs once per character and is active (LOW) during the sixth transmitter bit time, The signal is used in bit stream mode to time the transmitter step clock and has a duration of one bit time. Synchronize the oscilloscope on X BIT LAST and display several character times.

(6) Test Point 6. - The signal Transmitter Bit Time 1 (X BIT 1) occurs once per character and is active HIGH during the first transmitter bit time. The signal is used to generate the sample window signal and the X PL CLK timing signals. It has a duration of one bit time. Synchronize the oscilloscope on X BIT LAST and display several character times.

(7) Test Point 7. - The signal Sample Window (SMPL WDO) is active (HIGH) for the first two transmitter bit times in all start-stop modes and for the last half of the first bit time and the first half of the second bit time in bit stream mode. The signal is used to enable the start bit detector in start-stop modes and to enable the sample enable logic directly in bit stream. It has a duration of one or two bit times depending upon selected mode. Synchronize the oscilloscope on X BIT LAST and display several characters.

(8) Test Point 8. - The signal Transmitter Bit Last (X BIT LAST) occurs once per character and is active (LOW) during the last transmitter bit time. This signal is used to synchronize the whole transmitter, for it is during the last bit time that most of the data processing (including memory and encoding) takes place. It has a duration of one bit time. Self synchronize the oscilloscope and display several character times,

(9) Test Point a. - The signal Initialize 1 (INIT 1) is a negative-going 50 microsecond pulse that occurs 400 milliseconds after power turn on. It is the inverted pulse of the initialization signal INIT 1 generated by the dc-dc converter. It is active LOW only once, during the initialization sequence, and then remains constantly HIGH.

(10) Test Point b. - The output (Pin 4) of shift register U6 is the signal Transmitter Bit Time 2 (X BIT 2); it occurs once per character time and is active HIGH during the second transmitter bit time. The signal is used to generate the sample window signal and has a duration of one bit time. Synchronize the oscilloscope on X BIT LAST and display several characters.

(11) Test Point c. - The output (Pin 8) of inverter U8D is the signal Transmitter Bit Time 3 (X BIT 3). It occurs once per character time and is active LOW during the third transmitter bit time. The signal is used to deter-termine if the Sample Enable logic has been reset before the end of the transmitter third bit time. It has a duration of one bit time. Synchronize the oscilloscope on X BIT LAST and display several characters.

(12) Test Point d. - The output (Pin 9) of flip-flop U5B is the signal Transmitter Bit Time 6A (BIT). It occurs once per character time and is active LOW during the latter half of the sixth transmitter bit time and the first half of the seventh transmitter bit time. The signal is used to remove a glitch in the transmitter clock step signal X CLK ST L. It has a duration of one bit time. Synchronize the oscilloscope on X BIT LAST and display several characters.

5. Circuit Card Assembly A2A3, Transmitter Timing and Inhibit Logic. -

TP	1	Inhibit Activate or Deactivate Generator	INH A/D GEN
TP	2	Transmitter (Positive) Last Clock	X PL CLK
TP	3	Transmitter Clock Step (Data Source)	X CLK ST
TP	4	Transmitter (Positive) Clock	X P CLK
TP	5	Memory Write A	MEM WRITE A
TP	6	Transmitter (Negative) Last Clock	X NL CLK
TP	7	Transmitter Parallel-To-Serial Clock	X PS CLK
TP	8	Transmitter (Negative) Clock	X N CLK

(1) Test Point 1. - The signal Inhibit Activate or Deactivate Generate (INH A/D GEN) is active (LOW) during the initialization sequence and when the transmitter is inhibited from the distant end. It is not a periodic signal but is always enabled by the timing signal X PL CLK, which occurs at the

beginning of transmitter bit 1 time. The oscilloscope can be used to determine the logic level.

(2) Test Point 2. - The signal Transmitter (Positive) Last Clock (X PL CLK) occurs once per character time during the transmitter bit 1 time. The signal is normally HIGH; it has 3 microsecond negative-going pulses, which occur 3 microseconds after the trailing edge of the timing signal X P CLK, during the transmitter first bit time. Synchronize the oscilloscope on X BIT LAST and display several character times.

(3) Test Point 3. - The signal Transmitter Clock Step (X CLK ST) goes LOW to command a new character or data bit (depending upon selected mode) from the data source. In all start-stop modes it goes LOW for the first two transmitter bit times, but in bit stream mode it goes LOW six times in phase with the transmitter timing signal X CLK and commands one bit of new data with each fall. Synchronize the oscilloscope on X BIT LAST and display several character times.

(4) Test Point 4. - The signal Transmitter (Positive) Clock (X P CLK) occurs once per bit time and has a duration of 6 microseconds. The signal is normally HIGH and goes LOW for one period of the fast clock after the positive rise of the transmitter timing signal X CLK. Self-synchronize the oscilloscope and display several bit times.

(5) Test Point 5. - The signal Memory Write A (MEM WRITE A) occurs once per character time during the last half of the transmitter last bit time. It has a duration of 3 microseconds and occurs at least 3 microseconds after the Sample Enable Logic is preset. Synchronize the oscilloscope on X BIT LAST and display several character times.

(6) Test Point 6. - The signal Transmitter (Negative) Last Clock (X NL CLK) occurs once per character time during the transmitter last bit time. The signal is normally HIGH and has 3 microsecond negative-going pulses, which occur 3 microseconds after the leading edge of the timing signal X N CLK, at about the middle of the transmitter last bit time. Synchronize the oscilloscope on X BIT LAST and display several characters.

(7) Test Point 7. - The signal Transmitter Parallel-To-Serial Clock (X PS CLK) is normally HIGH with 3 microsecond negative -going pulses. During the transmitter last bit time this signal, which loads the parallel-to-serial converter, is delayed until 3 microseconds after the memory write signal; but during all other bit times it occurs 6 microseconds after the timing signal X P CLK. The X PS CLK occurs once per bit time but the last bit time pulse is delayed. Synchronize the oscilloscope on X BIT LAST and display several characters.

(8) Test Point 8. - The signal Transmitter (Negative) Clock (X N CLK) occurs once per bit time and has a duration of 6 microseconds. The signal is normally HIGH and goes LOW for one period of the fast clock after the fall of the transmitter timing signal X CLK. Self synchronize the oscilloscope and display several bit times.

(9) Test Point a. - The output (Pin 11) of NOR gate U20D is HIGH for the second half of the transmitter last bit time. It is during this time that the memory write pulse generator is enabled. Synchronize the oscilloscope on X BIT LAST and view several characters.

(10) Test Point b. - The signal Transmitter Last Parallel-To-Serial Clock (X LPS CLK) occurs once per character 3 microseconds after the memory write pulse. It is normally HIGH and consists of negative-going 3 microsecond pulses during the transmitter last bit time. Synchronize the oscilloscope on X BIT LAST and view several characters.

(11) Test Point c. - The signal Inhibit Supervisory Character Inhibit (INH SUP INH) is HIGH for one character time when either the Inhibit Activate or Inhibit Deactivate supervisory characters are transmitted. This signal holds the transmitter step clock to prevent a character being requested from the terminal source at the same time.

d. Circuit Card Assembly A2A4, Transmitter Sync and ARQ Control. -

TP	1	Transmitter Clear Sync Flags	X CL SYNC FLGS
TP	2	Transmitter Clear ARQ Flag	X CL ARQ FLG
TP	3	Memory ARQ Inhibit (write)	MEM ARQ INH
TP	4	Memory Input (bit) 10	MEM IN 10
TP	5	Memory Input (bit) 9	MEM IN 9
TP	6	Sync B Generate	SYNC B GEN
TP	7	Inhibit Activate or Deactivate Enable	INH A/D EN
TP	8	Sync A Generate	SYNC A GEN

(1) Test Point 1 - The signal Transmitter Clear SYNC Flags (X CL SYNC FLGS) is active LOW during part of the last character time of a SYNC cycle. The clear signal is LOW after the fall of the timing signal X NL CLK until the rise of the signal X L PS CLK (about 12 microseconds) near the center of the last bit time, during the last character of the SYNC cycle. The signal is only active if the transmitter has received the two SYNC flags from

the receiver and is leaving the SYNC cycle. Synchronize the oscilloscope on the timing signal X P CLK and view a single bit time.

(2) At Test Point 2. - The signal Transmitter Clear ARQ Flags (X CL ARQ FLG) is active LOW for the first two character times of an ARQ cycle. The clear signal is LOW after the rise of the signal X PL CLK (which is at the beginning of the first ARQ supervisory character that is transmitted) until the end of the second ARQ character transmitted. If the system is in a repeating ARQ cycle, the oscilloscope should be synchronized on MEM IN 9 and a whole ARQ cycle displayed.

(3) Test Point 3. - The signal Memory ARQ Inhibit (MEM ARQ INH) is active LOW during the ARQ cycle after transmitting the two ARQ supervisor characters until the end of the cycle. It inhibits the memory write command to the B memory and hence the transmitter retransmits the contents of each memory location. If the system is in a continuous ARQ cycle due to an error in synchronization, the signal can be monitored by synchronizing the oscilloscope on MEM IN 9 and displaying the whole ARQ cycle.

(4) Test Point 4. - The signal Memory Input 10 (MEM IN 10) is active HIGH for 12 microseconds during the last bit time of the character, prior to entering the SYNC cycle. lt is written into memory A by the write command signal MEM WRITE A, which is never inhibited and occurs during the 12 microseconds that MEM IN 10 is active. The signal marks the character before a SYNC cycle begins and is the character being processed when the resync command is given.

(5) Test Point 5. - The signal Memory Input 9 (MEM IN 9) is active HIGH for one character time. It is written into memory A by the write command signal MEM WRITE A, which is never inhibited and occurs during the time that MEM IN 9 is active. The signal marks the character before an ARQ cycle begins and is the character being processed when the ARQ command is given.

(6) Test Point 6. - The signal Sync B Generate (SYNC B GEN) is active LOW for the second character of a SYNC cycle. The memory output characters are disabled by X SYNCING and the signal SYNC B GEN forces the transmitter to transmit the supervisory character SYNC B. The signal is active LOW for one character time.

(7) Test Point 7. - The signal Inhibit Activate or Deactivate Enable (INH A/D EN) is active HIGH after the first two characters transmitted in a SYNC cycle until the end of the cycle. The memory output characters are disabled by X SYNCING and the signal INH A/D EN forces the transmitter to transmit Inhibit Activate or Inhibit Deactivate supervisory characters (dependent upon the inhibit switch or remote line) until the end of the sync cycle.

(8) Test Point 8. - The signal Sync A Generate (SYNC A GEN) is LOW for the first character of a SYNC cycle. The memory output characters are disabled by X SYNCING and the signal SYNC A GEN forces the transmitter to transmit the supervisory character SYNC A. The signal is active LOW for one character time.

(9) Test Point a. - The signal ARQ Sync Enable (ARQ SYNC EN) is HIGH for the duration of an ARQ cycle. The signal enables the operator to initiate a SYNC cycle.

(10) Test Point b. - The output (Pin 8) of the NOR gate U12C is LOW during the first two character times of an ARQ cycle to generate the two ARQ supervisory character that are transmitted before the characters in memory are retransmitted.

(11) Test Point c. - The signal Start SYNC Cycle ST SYNC CYCLE is LOW for one character time to initiate a transmitter SYNC cycle. The transmitter SYNC cycle can also be initiated by the receiver SYNC FLG 1 signal.

e. Circuit Card Assembly A2A5, Constant Ratio Code Generator. -

TP	1	Sample Counter (Binary input) 2	SMPL CTR 2
TP	2	Sample Counter (Binary input) 1	SMPL CTR 1
TP	3	Transmitter Send Line	SND LIN
TP	4	Sample Counter (Binary input 8	SMPL CTR 8
TP	5	8-BIT (SERIAL) DATA	8 BIT DA
TP	6	11 BIT DA	11 BIT DA
TP	7	Transmit Supervisory Character	X SUP OUT
TP	8	Sample Counter (Binary input) 4	SMPL CTR 4

(1) Test Point 1. - The signal Sample Counter 2 (SMPL CTR 2) depends upon the number of data bits to be sampled during each character. It forms the second binary bit of the number that is loaded into the Sample Enable Counter at the beginning of each character. The signal is a cons tan t logical level that can be monitored with the oscilloscope as HIGH or LOW and depends upon the input data format selected.

(2) Test Point 2. - The signal Sample Counter 1 (SMPL CTR 1) is identical to the signal at test point 1. It forms the first binary bit of the number that is loaded into the Sample Enable Counter.

(3) Test Point 3. - The signal Transmitter Send Line (SND LIN) is the output serialized constant ratio data code. Each output character is made up of 8 or 11 data bits (depending upon format selected) and has four 1's. The output signal is phased so that the data bits change at the rise of the transmitter timing signal X CLK, and are inverted by the line driver to generate the transmitter output signal SND LIN L. Synchronize the oscilloscope on X BIT LAST and display several character times to monitor the output I pattern.

(4) Test Point 4. - The signal Sample Counter 8 (SMPL CTR 8) signal is identical to the signal at test point 1. It forms the fourth binary bit of the number that is loaded into the Sample Enable Counter.

(5) Test Point 5. - The signal 8 Bit Data (8-BIT DA) is the first bit to be transmitted when bit stream or 5-bit start-stop formats are selected. It is not a start bit and can be 1 or 0 depending upon the character being transmitted. It is present at the test point after the Parallel-to-Serial Converter has been loaded during the transmitter last bit time by the timing signal X PS CLK. All the remaining bits of the output code are then shifted past the test point by successive pulses of the signal X PS CLK. Synchronize the oscilloscope on X BIT LAST and display several characters.

(6) Test Point 6. - The signal 11 Bit Data (11 BIT DA) is the first bit to be transmitted when 6, 7, or 8-bit start-stop formats are selected. The signal resembles that at Test 5 but is a longer code.

(7) Test Point 7. - The signal Transmit Supervisory Character (X SUP OUT) is HIGH for one character time if the supervisory character Idle, ARQ, Inhibit Activate, or Inhibit Deactivate are to be transmitted. The signal changes the outputs of the constant ratio encoders to generate the four extra constant ratio codes that are decoded by the receiver as supervisory characters.

(8) Test Point 8. - The signal Sample Counter 4 (SMPL CTR 4) is identical to the signal at test point 1; it forms the third binary bit of the number that is loaded into the Sample Enable Counter.

(9) Test Point a. - The signal Code 11 Bit (CODE 11 BIT) is HIGH if the transmitter is operating with an 11-bit constant ratio code--when the 6, 7, or 8-bit start-stop formats are selected.

(10) Test Point b. - The signal Code 8 Bit (CODE 8 BIT) is HIGH if the transmitter is operating with an 8-bit constant ratio code--when bit stream or S-bit start stop formats are selected.

f. Circuit Card Assembly A2A6, Data Input Code and Memory Address Counter. -

TP	1	Memory Address (Binary) 8	MEM ADD 8
TP	2	Transmitter Input Data Delayed	X IN DA DL
TP	3	Memory Input (Bit) 8	MEM IN 8
TP	4	Memory Chip Select 1	MEM CS 1
TP	5	Inhibit Activate Generate	INH ACT GEN
TP	6	ARQ Generate	ARQ GEN
TP	7	Inhibit Deactivate Generate	INH DEACT GEN
TP	8	Switch Inhibit Activate or Deactivate	SWITCH INH A/D

(1) Test Point 1. - The signal Memory Address 8 (MEM ADD 8) is the fourth binary memory address bit. The memory address counter is incremented once per character. Hence the signal MEM ADD 8 changes state every eighth character transmitted. If the memory length switch is set on position 0 or 1, this signal is a constant LOW. Synchronize the oscilloscope on MEM ADD MAX and display one memory length.

(2) Test Point 2. - The signal Transmitter Input Data Delayed (X IN DA DL) is the incoming data from the terminal source delayed 12 microseconds by the Start Bit Detector logic. The signal is used to check the center sampling of the serial-to-parallel converter. Synchronize the oscilloscope on X BIT LAST an&observe phase relationship between the signal X IN DA DL and the clock X SP CLK The clock pulses are only 3 microseconds wide.

(3) Test Point 3. - The signal Memory Input 8 (MEM IN 8) is the supervisory marker bit into the Memory A. It is HIGH after transmitter bit three, when a memorized supervisory character is to be transmitted. During an ARQ or SYNC cycle this test point is HIGH for all characters transmitted but is not written into memory because the memory write pulse is inhibited.

(4) Test Point 4. - The signal Memory Chip Select 1 (MEM CS 1) is LOW for the 16 memory addresses between 17 and 32, and HIGH for the remaining 48 addresses, The signal can be used to test the chip select decode logic synchronizing the oscilloscope on the signal MEM ADD MAX.

(5) Test Point 5. - The signal Inhibit Activate Generate (INH ACT GEN) is active LOW for one character time when the supervisory character Inhibit Activate is to be transmitted. The transmitter step clock-is inhibited; this prevents the sample enable logic being reset, and the Idle supervisor that would normally be transmitted is changed into the Inhibit Activate supervisor by the signal INH ACT GEN.

(6) Test Point 6. - The signal ARQ Generate (ARQ GEN) is active for one character time when the supervisory character ARQ is to be transmitted, Its function is similar to that described for test point 5.

(7) Test Point 7, - The signal Inhibit Deactivate Generate (INH DEACT GEN) is identical at test point 5. The Inhibit Deactivate supervisory character is transmitted.

(8) Test Point 8. - The signal Switch Inhibit Activate or Deactivate (SWITCH A/D) is if the front panel inhibit switch (or remote control line) is set for Inhibit ACTIVATE, and LOW when set for Inhibit DEACTIVATE. The signal controls which inhibit supervisory character is transmitted when the transmitter is inhibited from the distant end.

(9) Test Point a. - The output (Pin 6) of inverter U3C is LOW for one character time to generate the supervisory character Inhibit Deactivate.

(10) Test Point b. - The output (Pin 12) of inverter U3F is LOW for one character time to generate the supervisory character Inhibit ACTIVATE.

(11) Test Point c. - The output (Pin 8) of NAND gate U18 is LOW for one character time to generate the supervisory character Idle.

8. Circuit Card Assembly A2A7, Memory and Parity Logic. -

TP	1	Memory Output (Bit) 3	MEM OUT 3
TP	2	Memory Input (Bit) 3	MEM IN 3
TP	3	Parity Check	PAR CHK
TP	4	Memory Write B	MEM WRITE B
TP	5	Parity Bit Output	PARITY BIT OUT
TP	6	Memory Output (Bit) 9	MEM OUT 9
TP	7	Memory Output (Bit) 10	MEM OUT 10
TP	8	Memory Chip Select 0	MEM CS 0

(1) Test Point 1. - The signal Memory Output 3 (MEM OUT 3) is the third data bit stored in Memory B at the selected memory address. After a memory B write pulse it is identical to the memory input signal.

(2) Test Point 2. - The signal Memory Input 3 (MEM IN 3) is the third data bit to be stored in Memory B. It is not stored in the memory until after the memory write pulse.

(3) Test Point 3. - The signal Parity Check PAR CHK is HIGH if the parity checker found an error in parity on the output memory lines. This signal is tested 3 microseconds after a memory write signal, and disabled during an ARQ or SYNC cycle. Its function is to set a latch that lights a front panel indicator if a parity error is detected.

(4) Test Point 4. - The signal Memory Write B (MEM WRITE B) occurs once per character time during the last half of the transmitter last bit time. It has a duration of 3 microseconds and occurs at least 3 microseconds after the Sample Enable Logic is preset. It is disabled after the second character of an ARQ cycle and during the entire SYNC cycle. Synchronize the oscilloscope on X BIT LAST and display several character times.

(5) Test Point 5. - The signal Parity Bit Output PARITY BIT OUT is the signal generated by the parity generator after being stored in Memory A and inverted twice.

(6) Test Point 6. - The signal Memory Output 9 (MEM OUT 9) is the ARQ cycle marker bit after being stored in memory A. It is a LOW signal and can occupy only one memory address. It marks the beginning of a transmitter ARQ cycle. This bit is used to count the number of characters in the memory length selected that are retransmitted.

(7) Test Point 7. - The signal Memory Output 10 (MEM OUT 10) is the SYNC cycle marker bit after being stored in memory A. It is a LOW signal and can occupy only one memory address. It marks the beginning of a transmitter SYNC cycle. Like the ARQ marker bit MEM OUT 9 it is used as a counter to determine the number of characters required for one memory length.

(8) Test Point 8. - The signal Memory Chip Select 0 (MEM CS 0) is LOW for the first 16 memory addresses and HIGH for the remaining 48 addresses. The signal can be used to test the chip select logic.

h. Circuit Card Assembly A2A8, Line Receivers and Line Drivers. -

TP	1	Transmitter block (TTL)	X CLK
TP	2	Receiver block (TTL)	R CLK
TP	3	Receiver Input Data (TTL)	R IN DA
TP	4	Receiver Output Data (Bipolar)	R O DA L
TP	5	Receiver Clock Step (Bipolar)	R CLK ST L
TP	6	Transmitter Send Line (Bipolar)	SND LIN L

TP	7	Transmitter Clock Step (Bipolar)	X CLK ST L
TP	8	Output Signal Return	OUT SIG RTN

(1) Test Point 1. - The signal Transmitter Clock (X CLK) is the TTL compatible version of the externally provided transmitter clock. It has a period of one transmitter bit time (twice data rate) and controls the timing of the entire system. Synchronize the oscilloscope on X BIT LAST and display several character times.

(2) Test Point 2. - The signal Receiver Clock (R CLK) is the TTL compatible version of the externally provided receiver clock. It has a period of one data bit and is phased so that the incoming data bits change at the fall of R CLK (or rise of R CLK). It is used to control the receiver timing and need not have any fixed phase relationship with the transmitter clock. Synchronize the oscilloscope on R BIT LAST and display several character times.

(3) Test Point 3. - The signal Receiver Input Data (R IN DA) is the TTL compatible version of the received constant ratio code data from the distant transmitter. Each input character is made up of 8 or 11 data bits (depending upon format selected) and has four 1's, The incoming signal is phased so that the data bits change at the rise time of the receiver clock signal R CLK. Synchronize the oscilloscope on R BIT LAST and display several characters of the incoming data R IN DA and the receiver clock signal R CLK.

(4) Test Point 4. - The signal Receiver Output Data (R O DA L) is the output bipolar (±6 volts) signal to the terminal sink. In start-stop modes the first bit transmitted is a start bit (LOW) and the character is followed by two or more stop bits (HIGH). The character coding is identical to that received by the distant transmitter. In bit stream mode the output data consists of the six data bits accepted by the distant transmitter; the last bit is extended over three bit times to make up the eight bit times required to receive a character in bit stream. The data can be monitored by synchronizing the oscilloscope to the receiver R LAST BIT time and observing the I pattern.

(5) Test Point 5. - The signal Receiver Clock Step (R CLK ST L) is the output bipolar (±6 volts) signal to the terminal sink. It is a timing signal that is HIGH for one bit time and falls at the beginning of the start bit in all start-stop modes. It is six periods of the receiver clock that falls at the center of each output bit in bit stream mode. The oscilloscope should be synchronized to the R BIT LAST time and the clock step signal R CM ST L displayed with the receiver output data R O DA L.

(6) Test Point 6. - The signal Transmitter Send Line (SND LIN L) is the bipolar (±6 volts) output signal of the transmitter. Each output character is made up of 8 or 11 data bits (depending upon format selected) and has four

1's. The output is phased so that the data bits change state at the rise of the transmitter clock signal X CLK. Synchronize the oscilloscope on X BIT LAST and display several character times to monitor the I pattern.

(7) Test Point 7. - The signal Transmitter Clock Step (X CLK ST L) is the bipolar (±6 volt) signal to the terminal source. It goes HIGH to request a new character or data bit (depending upon selected mode) from the terminal source. In all start-stop modes it is HIGH for the first two transmitter bit times, but in bit stream mode it goes HIGH six times --in phase with the transmitter timing signal X CLK--and requests one bit of the new data for each rise. The transmitter step clock signal X CLK ST L is inhibited to transmit a supervisory character, and when the system enters an ARQ or SYNC cycle. Synchronize the oscilloscope on X BIT LAST and display several characters.

(8) Test Point 8. - The signal Output Signal Return (OUT SIG RTN) is the return line for the bipolar (±12 volt) power supply. It is connected to the TTL common in the dc-dc converter assembly.

(9) Test Point a. - The signal Transmitter Input Data (X IN DA) is the TTL compatible version of the incoming data from the terminal source, In start-stop modes the first bit received is a start bit, LOW, followed by the data bits of the character to be transmitted. In bit stream mode six data bits are received followed by two blank bit times. The data can be monitored by synchronizing the oscilloscope to the transmitter X BIT LAST time and observing the I pattern.

i. Circuit Card Assembly Card Assembly A2A9, Receiver Data Processor.

TP	1	Parallel-To-Serial (Bit) 1	P/S BIT 1
TP	2	Parallel-To-Serial (Bit) 5	P/S BIT 5
TP	3	Receiver Output Data A	R O DA A
TP	4	Check supervisory Received	CHK SUPP RCVD
TP	5	Unused Constant Ratio Code Received	UNUSED RCVD
TP	6	Constant Unused 11-Bit Constant Received	11 BIT UNUSED RCVD
TP	7	Receiver Input Data Delayed	R IN DA DL
TP	8	Nonconstant Ratio Code Received	NCR RCVD

(1) Test Point 1. - The signal Parallel/Serial Bit 1 (P/S BIT 1) is the first data bit transmitted to the data sink after the start bit in 8-bit start-stop

format and the start bit in 7-bit start-stop format. This occurs after the parallel-to-serial converter has been loaded during the receiver last bit time by the timing signal R N2 CLK--6 microseconds after the complete character has been decoded by the Constant Ratio Decoder. Each bit of the output terminal code is shifted past the test point with successive R N2 CLK clock pulses. The oscilloscope should be synchronized on R BIT LAST to monitor the I pattern.

(2) Test Point 2. - The signal Parallel/Serial Bit 5 (P/S BlT 5) is the third data bit to be transmitted to the data sink in bit stream format. It is like the signal at test point 1 except for bit position.

(3) Test Point 3. - The signal Receiver Output Data A (R O DA A) is the serial output data from the serial-to-parallel converter. The data is timed by the timing signal R X2 CLK, which occurs just after the center of each receiver bit time. When the receiver receives a supervisory character 01 enters and ARQ or SYNC cycle, this signal is held HIGH, which inhibits the data source. Synchronize the oscilloscope on the receiver R BIT LAST and observe several character times.

(4) Test Point 4. - The signal Check Supervisory Received (CHK SUPP RCVD) is HIGH receiver last bit time if four 1's have been received and R CODE 3 is one of the 1's. R CODE 3 is always HIGH when an ldle, ARQ lnhibit ACTIVATE, or Inhibit DEACTIVATE are received. If this signal is HIGH at last bit time. The receiver can fully decode the four supervisor characters by finding the bit position of the other three 1's.

(5) Test Point 5. - The signal Unused Constant Ratio Code Received (UNUSED RCVD) is HIGH at receiver last bit time if the constant ratio code received is unused (never transmitted) in the selected format. The signal is only useful during the receiver last bit time when the complete character is on the serial-to-parallel converter output lines, Synchronize the oscilloscope on R BIT LAST and display the two signal UNUSED RCVD and R BIT LAST.

(6) Test Point 6. - The signal Constant Unused 11-Bit Constant Ratio (11 BIT UNUSED RCVD) is LOW at receiver last bit time if the 11-bit constant ratio code received is one of the 68 codes that are not used, It is identical to and part of the signal at test point 5 and can be monitored in the same way.

(7) Test Point 7. - The signal Receiver lnput Data Delayed (R IN DA DL) is the incoming constant ratio code data from the distant transmitter clocked at the center of each data bit by the timing signal R CLK and hence delayed by half a bit time from the incoming data. Synchronize the oscilloscope on R BlT LAST and display several characters of the incoming data.

(8) Test Point 8. - The signal Nonconstant Ratio Code Received (NCR RCVD) is LOW at receiver last bit time if the character just received did not h have four 1's, and therefore is not a constant ratio code. Synchronize the oscilloscope on R BIT LAST and display the two signals NCR RCVD and R BIT LAST. If this signal is active (LOW) during last bit time, the receiver sets the ARQ flag.

(9) Test Point a. - The signal ARQ Received (ARQ RCVD) is LOW at receiver last bit time if the supervisory character ARQ is received.

(10) Test Point b. - The signal Inhibit Activate Received (INH ACT RCVD) is LOW at receiver last bit time if the supervisory character Inhibit ACTIVATE is received.

(11) Test Point c. - The signal Inhibit DEACTIVATE Received (INH DEACT RCVD) is LOW at receiver last bit time if the supervisory character Inhibit DEACTIVATE is received.

(12) Test Point d. - The signal IDLE Received (IDLE RCVD) is LOW at receiver last bit time if the supervisory character IDLE is received.

(13) Test Point e. - The signal Sync A Received (SYNC A RCVD) goes LOW when four consecutive l's are received. This signal starts a counter that reaches maximum count after one complete character.

(14) Test Point f. - The signal Sync B Received (SYNC B RCVD) goes LOW when the first four data lines out of the serial-to-parallel converter are 1's. This is a requirement for the supervisory character SYNC B.

(15) Test Point g. - The signal Sync 0 Received (SYNC 0 RCVD) goes LOW when the 8th, 9th, and 10th data lines out of the serial-to-parallel converter are 0's. This also is a requirement for the supervisory character SYNC B. When the signals SYNC B RCVD and SYNC 0 RCVD are both LOW, it is assumed that the supervisory character SYNC B is on the data lines. This can be at any receiver bit time.

j. Circuit Card Assembly A2A10, Receiver Control Logic. -

TP	1	Receiver Clock Step	R CLK ST
TP	2	Receiver (Negative 1) Clock	R N1 CLK
TP	3	Test Mode	$\overline{\text{TEST MODE}}$
TP	4	Receiver (Negative 2) Clock	R N2 CLK
TP	5	Receiver Last (Negative 2) Clock	R L N2 CLK

TP	6	Test Un-Sync	TEST UN -SYNC
TP	7	Receiver Bit (Time) Last	R BIT LAST
TP	8	Supervisory Character Received	SUPER RCVD

(1) Test Point 1. - The signal Receiver Clock Step (R CLK ST) goes fro from LOW to HIGH to inform the data sink that a new character or data bit (depending upon selected mode) is being transmitted on the data lines. In all start-stop modes a single pulse one bit wide indicates a new start bit but in bit stream six periods of the receiver clock indicate a new data bit at the rise of each clock period. Synchronize the oscilloscope on R BIT LAST and display several characters.

(2) Test Point 2. - The signal Receiver Negative 1 Clock (R N1 CLK) occurs once per bit time and has a duration of 3 microseconds. The signal is normally HIGH and goes LOW for the second half of one period of the fast clock after the negative fall of the receiver timing signal R CLK. Self-synchronize the oscilloscope and display several bit times.

(3) Test Point 3. - The signal Test Mode (TEST MODE) is LOW when the front panel TEST switch is in the ON position. It connects the TTL output signal of the local transmitter directly into the local receiver. The transmitter timing signal X CLK also becomes the receiver timing signal R CLK.

(4) Test Point 4. - The signal Receiver Negative 2 Clock (R N2 CLK) occurs once per bit time and has a duration of 3 microseconds. The signal is normally HIGH and goes LOW for the second half of the second period of the fast clock after the negative fall of the receiver signal R CLK. Hence this clock occurs 6 microseconds after the timing signal R N1 CLK. Self-synchronize the oscilloscope and display several bit times.

(5) Test Point 5. - The signal Receiver Last Negative 2 Clock (R L N2 CLK) occurs once per character time during the first 3 microseconds of receiver last bit time. The signal is normally HIGH with 3 microsecond negative-going pulses occurring at the same time as the time signal R N2 CLK--but only during last bit time. Synchronize the oscilloscope on R BIT LAST and display several character times.

(6) Test Point 6. - The signal Test Un-Sync (TEST UN-SYNC) is LOW for two character times if the system enters the TEST mode during the receiver last bit time. It prevents the system remaining in constant ARQ when the test mode is selected,

(7) Test Point 7. - The signal Receiver Bit Last (R BIT LAST) occurs once per character and is active HIGH during the last receiver bit time. This

signal is used to synchronize the whole receiver, for it is during the last bit time that most of the data processing takes place. During a SYNC cycle the absolute time of the signal R BIT LAST is shifted to be synchronous with the last bit time of the incoming data set by the distant transmitter. Self synchronize the oscilloscope and display several character times.

(8) Test Point 8. - The signal Supervisory Character Received (SUPER RCVD) is HIGH during the receiver last bit time if the supervisory characters ARQ, Inhibit ACTIVATE Inhibit DEACTIVATE, SYNC A, or SYNC B are received, or the system is processing a SYNC cycle. This signal inhibits the unused logic to prevent supervisory characters being declared unused. Synchronize the oscilloscope on R BIT LAST and display the two signals SUPER RCVD and R BIT LAST.

(9) Test Point a. - The signal Receiver Idle Data Inhibit (R IDL DA INH is LOW for one character time if the last character received is an Idle supervisor. It causes the receiver to output an all l's character code, but does not inhibit the receiver step clock signal.

(10) Test Point b. - The signal Receiver Output Enable (R OUT EN) is HIGH providing a supervisory character has not been received, or the system is not processing an ARQ or SYNC cycle. It enables normal data flow to the data sink.

k. Circuit Card Assembly A2A11, Receiver ARQ and SYNC Control. -

TP	1	Sync Pattern Counter Maximum Count	SYNC DET MAX CT
TP	2	Receiver Resynchronized	R RE-SYNC
TP	3	Receiver SYNC Counter Maximum Count	R SYNC MAX CT
TP	4	Receiver ARQ Counter Maximum Count	R ARQ MAX CT
T P	5	Receiver in Sync Cycle	R SYNCING
TP	6	Receiver Clock	R CLK 1
TP	7	Receiver ARQ Counter Skip on Resync	R ARQ CT SKP
TP	8	Receiver Last (Negative 1) Clock	R L N1 CLK

(1) Test Point 1. - The signal Sync Pattern Counter Maximum Count (SYNC DET MAX CT) is HIGH for one character time 8 or 11-bit times (depending upon format selected) after the signal SYNC A RCVD goes LOW. The counter counts up one complete character after receiving the signal

SYNC A RCVD and the logic tests for the signal SYNC B RCVD and SYNC 0 RCVD. The signal SYNC DET MAX CT goes HIGH one character time after any four consecutive 1's are received.

(2) Test Point 2. - The signal Receiver Resynchronized (R RE-SYNC) is LOW for one bit time if the signals SYNC B RCVD and SYNC 0 RCVD are both true (LOW) at the maximum count of Sync Pattern Counter (SYNC DET MAX CT) true (HIGH). This indicates that the unique resynchronization pattern has been received; the signal R RE-SYNC forces the present time to be receiver last bit time. This signal is not cyclic but the oscilloscope can be used to determine if it is being generated during a SYNC cycle.

(3) Test Point 3. - The signal Receiver SYNC Counter Maximum Count (R SYNC MAX CT) is HIGH for normal data flow. When the receiver enters a SYNC cycle, the signal goes LOW for two memory lengths minus two characters and repeats the receiver ARQ flag at the end of each ARQ cycle during this time. It also holds the SYNC cycle indicator on the transmitter lighted. During a repeating SYNC cycle, this signal is HIGH for one character time and can be used to synchronize the oscilloscope to monitor the characters transmitted or received during a complete SYNC cycle.

(4) Test Point 4. - The signal ARQ Counter Maximum Count (R ARQ MAX CT) is HIGH far normal data flow. When the receiver enters an ARQ cycle the signal goes LOW for one memory length, and inhibits the flow of data to the data sink for this time. During a repeating ARQ cycle this signal is HIGH for one character time and can be used to synchronize the oscilloscope to monitor the characters transmitted or received during a complete ARQ cycle. In the logic diagram this signal is also called ARQ CYCLE.

(5) Test Point 5. - The signal Receiver Sync Cycle (R SYNCING) is LOW when the receiver is processing a SYNC cycle.

(6) Test Point 6. - The signal Receiver Clock (R CLK) is the externally provided receiver clock signal. It has a period of one data bit and is phased so that the incoming data bits change at the rise of R CLK. Synchronize the oscilloscope an R BIT LAST and display several character times.

(7) Test Point 7. - The signal Receiver ARQ Counter Skip in Resync (R ARQ CT SKP) is LOW for the first half of every character received, and hence HIGH for the remainder of a character time. If the receiver is resynchronized during the first half of a character when the signal R ARQ CT SKP is LOW, the new receiver last bit time is not counted by the ARQ counter as a complete character; but if the resynchronization occurs during the last half of a character it is counted as a complete character.

(8) Test Point 8. - The signal Receiver Last Negative 1 Clock (R L N1 CLK) occurs once per character time during the last 3 microseconds of receiver last bit time. The signal is normally LOW with 3 microsecond positive-going pulses occurring at the same time as the timing signal R N1 CLK, but only during last bit time. Synchronize the oscilloscope on R BIT LAST and display several character times.

(9) Test Point a. - The signal Receiver ARQ Flag (R ARQ FLG) is HIGH from the time that the receiver detects an error or receives an ARQ supervisory character until the transmitter recognizes it. It can be from a few nanoseconds to a full character time depending upon the phase relationship between the receiver and transmitter.

(10) Test Point b. - The signal Receiver Inhibit Activate Flag (INH ACT FLG) is HIGH after the receiver has received the Inhibit ACTIVATE supervisory character and LOW after receiving Inhibit DEACTIVATE. It is not cleared by the transmitter at any time.

(11) Test Point c. - The signal Receiver SYNC Flag (R SYNC FLG 1) is LOW after the receiver has detected the resynchronize pattern until the end of the system SYNC cycle. This is at least two complete memory lengths

(12) Test Point d. - The signal Receiver SYNC Flag 2 (R SYNC FLG 2) is LOW after the receiver has resynchronized and then correctly received either the Inhibit ACTIVATE or the Inhibit DEACTIVATE supervisory character, until the end of the system SYNC cycle. This is at least two complete memory lengths.

Table 6-2. Transmitter Signal Name Glossary

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
$\overline{\text{ARQ GEN}}$	$\overline{\text{ARQ Supervisor}}$	A2A4P1-51	XMTR 25	XMTR 37	LOW for first two characters of transmitter "ARQ Cycle" to write and send "ARQ" Supervisory character twice.
$\overline{\text{ARQ IND}}$	$\overline{\text{ARQ Indicator}}$	A2A4P1-14	XMTR 25	XMTR 47	LOW during transmitter "ARQ Cycle" to activate ARQ IND L
$\overline{\text{ARQ IND FP}}$	$\overline{\text{ARQ Indicator Front Panel}}$	A2A4P1-18	XMTR 25	Front Panel	Same as above for front panel indicator.
ARQ IND L	ARQ Indicator Control Line	A2A8P1-34	XMTR 47	Terminal TB4-5	LOW level DC interface line MIL STD 188C
$\overline{\text{ARQ SUP INH}}$	$\overline{\text{ARQ Supervisory Character Inhibit}}$	A2A4P1-37	XMTR 25	XMTR 38	LOW after first two characters of transmitter "ARQ Cycle" to inhibit any further supervisory characters.
ARQ SYNC EN	ARQ SYNC Cycle Enable	---	XMTR 25	XMTR 26	HIGH during transmitter ARQ Cycle to enable manual initiation of SYNC Cycle.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
$\overline{\text{BIT STREAM}}$	$\overline{\text{Bit Stream}}$ Format	A2A1S2-5	Front Panel	XMTR 5 36 14 34 20	LOW when system format switch is in Bit Stream position
BIT STREAM	Bit Stream Format	A2A5P1-41	XMTR 34	XMTR 5	Complement of above.
CODE 8 BIT	8 Bit Constant Ratio Line Code	A2A5P1-26	XMTR 34	XMTR 16 33 32	HIGH when system format switch is in Bit Stream or 5 bit start-stop positions System will generate 8 Bit Constant Ratio Line Code.
CODE 11 BIT	11 Bit Constant Ratio	A2A5P1-28	XMTR 34	XMTR 16 33 32	HIGH when system format switch is in 6 Bit S-S or 7 Bit S-S or 8 Bit S-S positions. System generate 11 Bit Constant Ratio Line Code.
FAST CLK	Fast Clock	A2A2-P1-7	XMTR 12	XMTR 21 7 24 9 19 10 18 6	System crystal controlled clock (153.6 KHz).

Table 6-2 (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
$\overline{\text{FP INH ACT}}$	$\overline{\text{Front Panel Inhibit Activate}}$	A2A12S5-3	Front Panel	XMTR 23	Front panel switch line change from HIGH to LOW causes one inhibit activate supervisory character to be written and sent to distant receiver.
$\overline{\text{FP INH DEACT}}$	$\overline{\text{Front Panel Inhibit Deactivate}}$	A2A12S5-1	Front Panel	XMTR 23	Same as above for Inhibit Deactivate supervisory character.
FP SYNC INH	Front Panel Sync Inhibit	A2A4P1-35	XMTR 25	Front Panel	HIGH last character of transmitter ARQ cycle to inhibit front panel sync cycle initiation.
FP SYNC INT	Front Panel Sync Initiate	A2A12S3-1	Front Panel	XMTR 26	HIGH to initiate transmitter "SYNC Cycle" from front panel.
$\overline{\text{FP SYNC INT}}$	$\overline{\text{Front Panel Sync Initiate}}$	A2A12S3-3	Front Panel	XMTR 26	Complement of above.
$\overline{\text{INH ACT GEN}}$	$\overline{\text{Inhibit Activate Generate}}$	A2A3P1-53	XMTR 23	XMTR 38	LOW for one character time to write and send Inhibit Activate supervisory character.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
$\overline{\text{INH GEN}}$	$\overline{\text{Inhibit Generate}}$	A2A3P1-4	XMTR 22	XMTR 5 XMTR 38	LOW for one character time to write and send inhibit supervisory character selected on front panel switch.
INH A/D EN	Inhibit Activate or Deactivate Enable	A2A4P1-55	XMTR 28	XMTR 30	HIGH to enable inhibit supervisory character to be generated
$\overline{\text{INH A/D EN}}$	$\overline{\text{Inhibit Activate or Deactivate Enable}}$	---	XMTR 28	XMTR 27	Complement of above.
$\overline{\text{INH DEACT GEN}}$	$\overline{\text{Inhibit Deactivate Generate}}$	A2A3P1-55	XMTR 23	XMTR 38	LOW for one character time to write and send Inhibit Deactivate supervisory character.
$\overline{\text{INH REQ IND FP}}$	$\overline{\text{Inhibit Request Indicator Front Panel}}$	A2A3P1-5	XMTR 23	Front Panel	LOW to light front panel inhibit request indicator.
INH SUP INH	Inhibit Supervisor Inhibit	A2A3P1-57	XMTR 23	XMTR 11	HIGH for one character time during transmission on "Inhibit Activate" of "Inhibit Deactivate" to inhibit data source.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
INIT 1	Initialize One	A2A17-S1 J2-8	---	XMTR 13	HIGH Pulse (50) 500 millisec after power turn-on or after release of initialization switch
$\overline{\text{INIT 1}}$	$\overline{\text{Initialize One}}$	A2A2P1-16	XMTR13	XMTR 10 XMTR 15 XMTR 16 XMTR 39	Complement of above
$\overline{\text{INIT 2}}$	$\overline{\text{Initialize Two}}$	A2A2P1-9	XMTR 13	XMTR 23 22 25 27 28 38	LOW from "Init 1" until "Mem Add Max" occurs (one memory cycle + 4 characters) causes Inhibit Activate supervisory characters to be loaded into all memory addresses before accepting data from source.
INIT 3	Initialize Three	A2A2P1-20	XMTR 13	XMTR 33	LOW from "Init 1" until first memory write pulse "Mem Write A" prevents random data being transmitted by power turn-on.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
LOCAL INH	Local Inhibit	A2A8P1-13	XMTR 4	XMTR 23	LOW from line receiver to cause "Inhibit Activate" supervisor to be written and sent from remote line.
LOCAL END INH L	Lock Inhibit Control Line	A2A14TB4-2	Terminal TB4-2	XMTR 4	Control line interface by LOW level DC - MIL STD 188C.
LOCAL END INH LR	Lock Inhibit Return Line	A2A14/TB4-1	TB4-1	XMTR 4	Return line for above.
MEM ADD MAX	Memory Address Counter Maximum Count	A2A6P1-14	XMTR 39	XMTR 13	LOW for four character times starting when memory address counter has maximum count.
MEM ADD 1	Memory Address Lines (64 memory locations)	A2A6P1-20	XMTR 35	XMTR 40, 41	Memory Address Lines 6 Bit Binary Address of selected memory location.
MEM ADD 2		A2A6P1-25	XMTR 35	XMTR 40, 41	
MEM ADD 4		A2A6P1-27	XMTR 35	XMTR 40, 41	
MEM ADD 8		A2A6P1-29	XMTR 35	XMTR 40, 41	
MEM ADD 16		A2A6P1-51	XMTR 35	XMTR 41	
MEM ADD 32		A2A6P1-53	XMTR 35	XMTR 41	
MEM CS 0	Memory Address Chip Select	A2A6P1-46	XMTR 35	XMTR 40, 41	Memory Chip Select - one out of four LOW to enable "Memory Chips" containing address required.
MEM CS 1		A2A6P1-48	XMTR 35	XMTR 40, 41	
MEM CS 2		A2A6P1-44	XMTR 35	XMTR 40, 41	
MEM CS 3		A2A6P1-50	XMTR 35	XMTR 40, 41	

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
					Derived from two most significant bits of memory address counter output
MEM ARQ INH	Memory ARQ Inhibit	A2A4P1-6	XMTR 25	XMTR 38 XMTR 43	LOW during all but first two character times of transmitter "ARQ cycle" prevents memory being changed if transmitter is in "ARQ cycle".
MEM IN 0	Memory "B"	A2A6P1-49	XMTR 37	XMTR 41	Memory Data Input Lines
MEM IN 1	Input Lines	A2A6P1-56	XMTR 37	XMTR 41	MEM IN 0 MEM IN 7
MEM IN 2		A2A6P1-13	XMTR 37	XMTR 41	are Input Terminal Data
MEM IN 3	(9 parallel lines)	A2A6P1-54	XMTR 37	XMTR 41	Bits. MEM IN 8 - High
MEM IN 4		A2A6P1-10	XMTR 37	XMTR 41	for supervisory control
MEM IN 5		A2A6P1-12	XMTR 37	XMTR 41	characters.
MEM IN 6		A2A6P1-15	XMTR 37	XMTR 41	
MEM IN 7		A2A6P1-6	XMTR 37	XMTR 41	
MEM IN 8		A2A6P1-19	XMTR 38	XMTR 41	

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
MEM IN 9	Memory "A" Input Lines (3 parallel lines)	A2A4P1-33	XMTR 25	XMTR 40	MEM IN 9 - HIGH for start of transmitter "ARQ cycle"
MEM IN 10		A2A4P1-19	XMTR 27	XMTR 40	MEM IN 10 - HIGH for start of transmitter "sync cycle".
MEM IN 11		---	XMTR 42	XMTR 40	MEM IN 11 - Memory Parity Bit.
MEM WRITE A	Memory Write A	A2A3P1-27	XMTR 24	XMTR 38	HIGH Pulse (3 micro sec) during transmitter last bit time to load data and markers into memory. Also used to derive Mem Write B.
$\overline{\text{MEM WRITE A}}$	$\overline{\text{Memory Write A}}$	A2A3P1-32	XMTR 24	XMTR 13 XMTR 40	LOW Pulse (3 micro sec) during transmitter last bit time to load "ARQ cycle" or "Sync cycle" markers.
$\overline{\text{MEM WRITE B}}$	$\overline{\text{Memory Write B}}$	A2A6P1-43	XMTR 38	XMTR 41	LOW Pulse (3 micro sec) at same time as "Mem Write A" but gated by Mem ARQ Inh to prevent Memory B being changed during "ARQ cycle".

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
MEM LG 4 MEM LG 8 MEM LG 16 MEM LG 32	Memory Length Switch (4 bit binary)	A2A12S1D-1 A2A12S1D-2 A2A12S1D-3 A2A12S1D-4	Front Panel Front Panel Front Panel Front Panel	XMTR 39 XMTR 39 XMTR 39 XMTR 39	Mem Lg 4 - Mem Lg 32 are four binary coded lines from Memory Length Switch on set-up control panel, giving control of recirculating memory length.
MEM LG + V	Memory Length Switch plus Voltage	A2A2P1-43			MEM LG + V - HIGH through limiting resistor to memory length switch.
$\overline{\text{PAR FAIL IND FP}}$	$\overline{\text{Parity Fail Indicator Front Panel}}$	A2A7P1-30	XMTR 43	Front Panel	LOW until reset if memory parity fails to light indicator on front panel.
$\overline{\text{PAR FAIL RES}}$	$\overline{\text{Parity Fail Reset}}$	A2A12S4-3	Front Panel	XMTR 43	LOW when reset switch is depressed to reset parity failure indicator.
R ARQ FLG	Receiver ARQ Flag	A2A11P1-53	RCVR 26	XMTR 25	HIGH when receiver has received mutilated character and requests ARQ cycle.

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Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
R INH ACT FLG	Receiver Inhibit Activate Flag	A2A11P1-24	RCVR 27	XMTR 22	HIGH when receiver has received "Inhibit Activate" supervisory character to request transmitter inhibit dependent upon "strap option".
R SYNC FLG 1	Receiver Sync Flag (One)	A2A11P1-32	RCVR 28	XMTR 27	LOW when receiver has received sync pattern request transmitter to enter "sync cycle".
R SYNC FLG 2	Receiver Sync Flag (Two)	A2A11P1-20	RCVR 28	XMTR 27	LOW when receiver has received sync pattern followed by inhibit deactivate or activate character.
R SYNCING	Receiver Syncing	A2A11P1-46	RCVR 25	XMTR 27	LOW when receiver is in "sync cycle".
R DIST INH IND	Received Distant Inhibit Indicator	A2A3P1-8	XMTR 22	XMTR 48	LOW when last inhibit supervisory character received was "Inhibit Activate" - drives line driver to give remote indication.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R DIST INH IND FP	Received Distant Inhibit Indicator Front Panel	A2A3P1-10	XMTR 22	Front Panel	Same as above for Front Panel.
R DIST INH L	Distant Inhibit Indicator Control Line	A2A8P1-30	XMTR 48	Terminal TB5-6	Control line to distant indicator LOW level DC interface MIL STD 188C.
SMPL WDO	Sample Window	A2A2P1-5	XMTR 14	XMTR 5	HIGH during time that new input data (source) may be accepted (X bit 1 delayed in Bit Stream and X Bit 1 and X bit 2 in Start-Stop modes).
SMPL CTR LD	Sample Counter Load	---	XMTR 10	XMTR 10	LOW to load sample bit counter at beginning new character.
SMPL ADJ 0	Bit Stream Center Sample Adjustment (12 binary bits)	A2A12S1C-1	Front Panel	XMTR 9	Center Sampling adjustment for Bit Stream Mode. 3 hexadecimal switches located on set-up panel adjust timing for center sampling of Bit Stream data. Each position of switch represents one fast clock period or about 6 micro secs.
SMPL ADJ 1		A2A12S1C-2	"	"	
SMPL ADJ 2		A2A12S1C-4	"	"	
SMPL ADJ 3		A2A12S1C-8	"	"	
SMPL ADJ 4		A2A12S1B-1	"	"	
SMPL ADJ 5		A2A12S1B-2	"	"	
SMPL ADJ 6		A2A12S1B-4	"	"	
SMPL ADJ 7		A2A12S1B-8	"	"	
SMPL ADJ 8		A2A12S1B-1	"	"	

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
SMPL ADJ 9		A2A12S1B-2	Front Panel	XMTR 9	
SMPL ADJ 10		A2A12S1B-4	"	"	
SMPL ADJ 11		A2A12S1B-8	"	"	
SMPL ADJ + V0	Center Sample	A2A2P1-45			HIGH through limiting resistor to bias common terminal of switches.
SMPL ADJ + V4	Switch plus	A2A2P1-47			
SMPL ADJ + V8	Voltage	A2A2P1-49			
SMPL CTR 1	Sample Bit	A2A5P1-17	XMTR 34	XMTR 10	Format Control 4 bit code derived from system mode switch (set-up panel) to determine number input data bits per character.
SMPL CTR 2	Counter Input	A2A5P1-22	XMTR 34	XMTR 10	
SMPL CTR 4		A2A5P1-52	XMTR 34	XMTR 10	
SMPL CTR 8		A2A5P1-8	XMTR 34	XMTR 10	
$\overline{\text{SND LIN}}$	$\overline{\text{Send Line}}$	A2A5P1-14	XMTR 33	XMTR 44	Transmitter output line code 8 or 11 bits per word continuous
SND LIN L	Send Line	A2A8P1-40	XMTR 44	Terminal TB5-1	Transmitter output LOW level DC interface - MIL STD 188C.
$\overline{\text{SYNC A GEN}}$	$\overline{\text{Sync A Generate}}$	A2A4P1-53	XMTR 28	XMTR 32	LOW for one character time to generate supervisory Sync A. Note: - This is not stored in memory.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
$\overline{\text{SYNC B GEN}}$	$\overline{\text{Sync B Generate}}$	A2A4P1-57	XMTR 28	XMTR 32	LOW for one character time to generate supervisory Sync B. Note: - This is not stored in memory.
$\overline{\text{SYNC IND}}$	$\overline{\text{Sync Cycle Indicator}}$	A2A4P1-12	XMTR 27	XMTR 45	LOW to line driver to cause remote "sync indicator" to light.
$\overline{\text{SYNC IND FP}}$	$\overline{\text{Sync Cycle Indicator Front Panel}}$	A2A4P1-20	XMTR 27	Front Panel	Same as above for front panel.
SYNC IND L	Sync Cycle Indicator Control Line	A2A8P1-36	XMTR 45	Terminal TB4-8	Control line to distant sync indicator LOW level DC interface - MIL STD 188C.
$\overline{\text{SYNC INT}}$	$\overline{\text{Sync Initiate}}$	A2A8P1-19	XMTR 3	XMTR 26	LOW to initiate transmitter "sync cycle" output of line receiver from remote switch.
SYNC INT L	Sync Initiate Control	A2A14TB4-3	Terminal	XMTR 3	Control line from distant sync initiate switch LOW level DC interface - MIL STD 188C.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
INH SWITCH A/D	Inhibit Switch Activate/Deactivate	A2A3P1-44	XMTR 23	XMTR 38	HIGH to generate "Inhibit Activate" LOW to generate "Inhibit Deactivate" supervisory characters when enabled by INH GEN or INH A/D EN
$\overline{\text{ST SYNC CYCLE}}$	$\overline{\text{Start Sync Cycle}}$	---	XMTR 26	XMTR 27	LOW to initiate sync cycle from local end.
$\overline{\text{X ARQ INH}}$	$\overline{\text{Transmitter ARQ Inhibit}}$	A2A4P1-31	XMTR 25	XMTR 11 XMTR 23	LOW during transmitter "ARQ cycle" to inhibit transmitter step clock and inhibit operation.
X BIT CODE 0	Transmitter	---	XMTR 35	XMTR 36, 37	Input data terminal (source) code in parallel format; number data bits used dependent upon input format (6 or 7 or 8). In 5 bits S-S, 6 bit S-S and 7 bit S-S, the start bit is considered as part of "data code" in the transmitter and receiver.
X BIT CODE 1	Input Source	---	"	"	
X BIT CODE 2	Code	---	"	"	
X BIT CODE 3		---	"	"	
X BIT CODE 4	(Parallel Format)	---	"	"	
X BIT CODE 5		---	"	"	
X BIT CODE 6		---	"	"	
X BIT CODE 7		---	"	"	

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X BIT 1	Transmitter Bit Time 1	A2A2P1-38	XMTR 15	XMTR 19 XMTR 14	HIGH during first count of transmitter bit counter time of first bit of constant ratio output code.
X BIT 2	Transmitter Bit Time 2	A2A2P1-36	XMTR 15	XMTR 20 XMTR 14	HIGH during second count of transmitter bit counter.
$\overline{\text{X BIT 3}}$	$\overline{\text{Transmitter Bit Time 3}}$	A2A2P1-34	XMTR 15	XMTR 38	LOW during third count of transmitter bit counter.
$\overline{\text{X BIT 6}}$	$\overline{\text{Transmitter Bit Time 6}}$	A2A2P1-3	XMTR 15	XMTR 20	LOW during sixth count of transmitter bit counter.
$\overline{\text{X BIT 6A}}$	$\overline{\text{Transmitter Bit Time 6A}}$	A2A2P1-26	XMTR 17	XMTR 20	Re-timed $\overline{\text{X BIT 6A}}$ to deglitch output blanking.
X BIT LAST	Transmitter Last Bit	A2A2P1-11	XMTR 16	XMTR 19 XMTR 20 XMTR 21	HIGH during last count of transmitter bit counter.
$\overline{\text{X BIT LAST}}$	$\overline{\text{Transmitter Last Bit}}$	A2A2P1-13	XMTR 16	XMTR 21 XMTR 33	Complement of above.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X CODE 0	Transmitter	---	XMTR 31	XMTR 32, 33	Transmitter output constant ratio code in parallel format 8 or 11 bits used dependent upon data format switch. Output is continuous data bits.
X CODE 1	Constant Ratio	---	"	"	
X CODE 2	Output Code	---	"	"	
X CODE 3	(parallel format)	---	"	"	
X CODE 4		---	"	"	
X CODE 5		---	"	"	
X CODE 6		---	"	"	
X CODE 7		---	"	"	
X CODE 8		---	"	"	
X CODE 9		---	"	"	
X CODE 10		---	"	"	
X CLK-1	Transmitter Clock	A2A3P1-41	XMTR 18	XMTR 18 XMTR 23 XMTR 20 XMTR 22 XMTR 33	Station transmitter clock external signal at 2 x data rate. Output constant ratio code bits change on rise of X CLK. Input data from terminal is delayed to maximum of 2 complete cycles of X CLK.
$\overline{\text{X CLK}}$	$\overline{\text{Transmitter Clock}}$	A2A8P1-7	XMTR 2	XMTR 18	Complement of X CLK.
$\overline{\text{X CLK-1}}$	$\overline{\text{Transmitter Clock-1}}$	A2A3P1-18	XMTR 23	XMTR 17 XMTR 26 XMTR 27	Buffered transmitter clock

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X CLK L	Transmitter Clock Line	A2A14TB3-4	Terminal TB3-4	XMTR 2	Station transmitter clock line LOW Level DC interface - MIL STD 188C.
X CLK LR	Transmitter Clock Line Return	A2A14TB3-3	---	XMTR 2	Return line for above.
X CLK ST	Transmitter Clock Step	A2A3P1-7	XMTR 20	XMTR 46	Complement of Transmitter Step Clock to input data terminal (source) Start-Stop one step two bits duration once per character. Bit Stream one cycle per bit time (six per character).
X CLK ST L	Transmitter Clock	A2A8P1-28	XMTR 46	Terminal TB5-2	Input Data Control Clock step output line. LOW level DC interface. MIL STD 188C.
X P CLK	Transmitter Positive (Rise) Clock	---	XMTR 18	XMTR 19	HIGH Going Pulses (6 microsecs) after rise of station transmitter clock.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X P CLK DL	Transmitter Positive (Rise) Clock Delayed	---	XMTR 19	XMTR 21	HIGH Going Pulses (6 microsecs) delayed one fast clock period (6 microsecs) after X P CLK
$\overline{\text{X P CLK}}$	Transmitter Positive (Rise) Clock	A2A3P1-36	XMTR 18	XMTR 9 XMTR 15 XMTR 16 XMTR 24	Complement of X P CLK
X N CLK	Transmitter Negative (Fall) Clock	---	XMTR 18	XMTR 19	HIGH Going Pulses (6 microsecs) after fall of station transmitter clock.
$\overline{\text{X N CLK}}$	Transmitter Negative (Fall) Clock	A2A3P1-38	XMTR 18	XMTR 7, 8 XMTR 14	Complement of above.
X PL CLK	Transmitter Positive (Rise) Last Clock	A2A3P1-21	XMTR 19	XMTR 25 XMTR 28 XMTR 39	HIGH Going Pulses (3 microsecs) after rise of station transmitter clock during last bit time.
X SMPL CTR CLK	Transmitter Sample Counter Clock	---	XMTR 6	XMTR 10	Gated fast clock to sample bit counter.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X NL CLK	Transmitter Negative (Fall) Last Clock	A2A3P1-17	XMTR 19	XMTR 25 XMTR 26 XMTR 27	HIGH Going Pulses (3 microsec) after fall of station transmitter clock during X BIT 1 Time.
X NL CLK	Transmitter Negative (Fall) Last Clock	A2A3P1-19	XMTR 19	XMTR 24 XMTR 22	Complement of above.
$\overline{\text{X SP CLK}}$	Transmitter Serial to Parallel Clock	A2A1P1-11	XMTR 6	XMTR 35	LOW Going Pulses (3 microsec) at center of each input terminal (source) data bit used to clock serial input data into shift register to form parallel character code.
$\overline{\text{X PS CLK}}$	Transmitter Parallel to Serial Clock	A2A3P1-42	XMTR 21	XMTR 33	LOW Going Pulses (3 microsec) occurs one fast clock (6 microsec) after X P CLK except during last bit time when it occurs 3 microsec after MEM WRITE A.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X L PS CLK	Transmitter Parallel to Serial Last Clock	A2A3P1-40	XMTR 21	XMTR 23	LOW Going Pulses (3 microsec) wide occurring 3 microsec after MEM WRITE A.
X SP CLK TM	Transmitter Serial to Parallel Clock Time	---	XMTR 8	XMTR 6 XMTR 10	HIGH Going Pulses (3 microsec) wide at serial to parallel clock time.
X DA INH RCVD	Transmitter Data Inhibit Received	A2A3P1-50	XMTR 22	XMTR 11	LOW to inhibit data terminal (source) when "Inhibit Activate" character received and inhibit option A is selected.
X ST BIT DET	Transmitter Start Bit Detected	---	XMTR 5	XMTR 9	LOW to hold sample counter when start bit detected Start-Stop modes (not used in Bit Stream).
X ST SMPL EN	Transmitter Start Sample En Enable	---	XMTR 5	XMTR 10	HIGH to enable transmitter "Sample Enable Latch".
X DA SMPL EN	Transmitter Data Sample Enable	A2A1P1-23	XMTR 10	XMTR 6	HIGH to enable transmitter to accept new data character bits from terminal (source).

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
X DA SMPL EN	Transmitter Data Sample Enable	A2A1P1-58	XMTR 10	XMTR 9 XMTR 24 XMTR 38	Complement of X DA SMPL EN
X IN DA INH	Transmitter Input Data Inhibit	A2A1P1-45	XMTR 11	XMTR 10 XMTR 20	LOW to inhibit data from input terminal (source).
X DA/SUP	Transmitter Data/Supervisor	---	XMTR 38	XMTR 36	HIGH - to transmit data LOW - to transmit memorized supervisor characters.
X SYNCING	Transmitter in "Sync Cycle"	A2A4P1-8	XMTR 27	XMTR 11 XMTR 23 XMTR 29	LOW during transmitter "sync cycle" to inhibit data from source and step
X CL ARQ FLG	Transmitter Clear ARQ Flag	A2A4P1-4	XMTR 25	RCVR 26	LOW for first two characters of transmitter "ARQ cycle" to clear receiver flag.
X CL SYNC FLGS	Transmitter Clear Sync Flags	A2A4P1-10	XMTR 27	RCVR 28	LOW for last character of transmitter "sync cycle" to clear receiver flags.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X IN DA L	Transmitter Input Data Line	A2A14TB3-1	Terminal TB3-1	XMTR 1	Input terminal (source) data line LOW level DC interface MIL STD 188C.
X IN DA LR	Transmitter Input Data Return Line	A2A14TB3-2	Terminal TB3-2	XMTR 1	Return line for above.
X IN DA	Transmitter Input Data	A2A8P1-35	XMTR 1	XMTR 5	Input Data from terminal (source) after level conversion.
X IN DA DL	Transmitter Input Data Delayed	A2A1P1-57	XMTR 5	XMTR 35	Input Data delayed (12 microsec) (2 fast clock periods).
$\overline{\text{5 BIT S-S}}$	$\overline{\text{5 Bit Start-Stop}}$	A2A12S2-1	Front Panel	XMTR 34 XMTR 36	LOW when format switch on set-up panel is set to 5 Bit Start-Stop.
6 BIT S-S	6 Bit Start-Stop	A2A12S2-2	Front Panel	XMTR 34 XMTR 36	LOW when format switch on set-up panel is set to 6 Bit Start-Stop.

Table 6-2. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
$\overline{\text{7 BIT S-S}}$	$\overline{\text{7 Bit Start-Stop}}$	A2A12S2-3	Front Panel	XMTR 34	LOW when format switch on set-up panel is set to 7 Bit Start-Stop.
$\overline{\text{8 BIT S-S}}$	$\overline{\text{8 Bit Start-Stop}}$	A2A12S2-4	Front Panel	XMTR 34	LOW when format switch on set-up panel is set to 8 Bit Start-Stop.

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Table 6-3. Receiver Signal Name Glossary

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
$\overline{\text{ARQ RCVD}}$	$\overline{\text{ARQ Super Received}}$	A2A9P1-5	RCVR 15	RCVR 10	LOW during last bit time if $\overline{\text{ARQ}}$ supervisory character being received.
$\overline{\text{ARQ CYCLE}}$	$\overline{\text{ARQ Cycle}}$	---	RCVR 24	RCVR 25 RCVR 24 RCVR 26 RCVR 20 RCVR 22	LOW during receiver ARQ cycle.
$\overline{\text{BIT STREAM}}$	$\overline{\text{Bit Stream Format}}$	A2A12S2-5	Front Panel	RCVR 9	LOW when system format switch on set-up panel is in "Bit Stream" position.
CODE 8 BIT	8 Bit Line Code	A2A5P1-26	XMTR	RCVR 15 RCVR 18 RCVR 5 RCVR 8 RCVR 21	HIGH when system format switch on set-up panel is in "Bit Stream" or "5 Bit Start Stop" to generate 8 bit constant ratio line code
CODE 11 BIT	11 Bit Line Code	A2A5P1-28	XMTR	RCVR 14 RCVR 16 RCVR 5 RCVR 8 RCVR 21	HIGH when system format switch on set-up panel is in "6 Bit S-S" or "7 Bit S-S" or "8 Bit S-S" to generate 11 bit constant ratio line code.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
FAST CLK	Fast Clock	A2A2P1-7	XMTR	RCVR 4	Internal Master Crystal Clock (153.6 KHz)
$\overline{\text{FORCE RCVR LAST BIT}}$	Force Last Bit	---	RCVR 6	RCVR 5	LOW pulse after selection of test "Mode" force system out of synchronization.
$\overline{\text{IDLE RCVD}}$	$\overline{\text{Idle Super Received}}$	A2A9P1-7	RCVR 15	RCVR 10	LOW during last bit time if idle supervisory character being received.
INH ACT FLG	Inhibit Activate Flag	A2A11P1-24	RCVR 27	XMTR	HIGH from receiving "Inhibit Activate" supervisor until "Inhibit Deactivate" is received. Used to indicate and optionally inhibit the transmitter.
$\overline{\text{INH ACT RCVD}}$	$\overline{\text{Inhibit Activate Received}}$	A2A9P1-9	RCVR 15	RCVR 10 RCVR 27 RCVR 28	LOW during last bit time if Inhibit Activate supervisory character being received.
$\overline{\text{INH DEACT RCVD}}$	$\overline{\text{Inhibit Deactivate Received}}$	A2A9P1-11	RCVR 15	RCVR 10 RCVR 27 RCVR 28	LOW during last bit time if Inhibit Deactivate supervisory character being received.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
INIT 1-1	Initialize One	Generated from INIT 1	---	RCVR 22 RCVR 21	HIGH pulse (50 microsec) 500 milliseconds after power turn-on or upon release of initialization switch.
$\overline{\text{INIT 1}}$	$\overline{\text{Initialize One}}$	A2A2P1-16	XMTR	RCVR 6 RCVR 5 RCVR 9 RCVR 10 RCVR 20 RCVR 23 RCVR 25 RCVR 27 RCVR 28 RCVR 21 RCVR 24	Complement of above.
$\overline{\text{MC IND}}$	$\overline{\text{Mutilated Character Indicator}}$	A2A11P1-55	RCVR 20	RCVR 30	LOW to Line Driver to activate Remote Mutilated Character Indicator.
MC IND L	Mutilated Character	A2A8P1-42	RCVR 30	Terminal TB4-7	HIGH to Remote Indicator.
MC IND FP	Mutilated Character Indicator Front Panel	A2A11P1-54	RCVR 20	Front Panel	Active LOW to light M. C. indicator on front panel.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
NCR RCVD	Non-Constant Ratio Character Received	A2A9P1-S8	RCVR 13	RCVR 20 RCVR 26 RCVR 15	LOW during last bit time if character being received is not a Constant Ratio Code (Does not have 4 one's)
MEM LG 4 MEM LG 8 MEM LG 16 MEM LG 32	Memory Length Switch (Binary)	A2A12S1 D-1 A2A12S1 D-2 A2A12S1 D-4 A2A12S1 D-8	Front Panel	RCVR 23 RCVR 23 RCVR 23 RCVR 23	Four bit binary output of memory length switch on set-up panel to control length of recirculating memory. Max length 64 characters.
MEM LG 4+INZ MEM LG 8+INZ MEM LG 16+INZ MEM LG 32+INZ	Memory Length Switch ORed to Initialize Pulse	--- --- --- ---	RCVR 23	RCVR 24, 25 RCVR 24, 25 RCVR 24, 25 RCVR 24, 25	Memory length switch binary output forced HIGH by initialization pulse.
R ARQ CT SKP	Receiver ARQ Counter Skip	A2A10P1-12	RCVR 8	RCVR 24	LOW during first half of receiver bit counter causes receiver ARQ counter to skip count if resync occurs when LOW.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R CODE 0	Received Con-	---	RCVR 14	RCVR15,16,17	Used to detect supervisory
R CODE 1	stant Ratio Code		RCVR 14	"	characters and unused
R CODE 2	Bits 0-10 in Par-		RCVR 14	"	constant ratio codes De-
R CODE 3	allel Format		RCVR 14	"	coded into Terminal Codes
R CODE 4			RCVR 14	"	R BIT 0 thru R BIT 7 for
R CODE 5			RCVR 14	"	Data Sink.
R CODE 6			RCVR 14	"	
R CODE 7			RCVR 14	"	
R CODE 8			RCVR 14	"	
R CODE 9			RCVR 14	"	
R CODE 10			RCVR 14	"	
$\overline{\text{RECODE 1}}$	Decoded	---	RCVR 16	RCVR 15	Used to generate $\overline{\text{R SYNC 0}}$
$\overline{\text{RECODE 2}}$	Terminal		RCVR 16	RCVR 15	
$\overline{\text{RECODE 3}}$			RCVR 16	RCVR 15	
R BIT 0	Decoded Ter-	---	RCVR 17	RCVR 18	Used by parallel to serial
R BIT 1	minal Codes		RCVR 17	RCVR 18	converter to generate out-
R BIT 2	Parallel Format		RCVR 17	RCVR 18	put serial data to the data
R BIT 3			RCVR 17	RCVR 18	SINK.
R BIT 4			RCVR 17	RCVR 18	
R BIT 5			RCVR 17	RCVR 18	
R BIT 6			RCVR 17	RCVR 18	
R BIT 7			RCVR 17	RCVR 18	

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R BIT CT 1 R BIT CT 2 R BIT CT 4 R BIT CT 8	Receiver Character Bit Counter (Binary Output)	---	RCVR 5 RCVR 5 RCVR 5 RCVR 5	RCVR 8, 9 RCVR 8, 9 RCVR 8, 9 RCVR 8, 9	Received character bit times used to generate Receiver Clock Step $\overline{R}$ $\overline{CLK\ ST}$ and the $\overline{ARQ\ CT\ SKP}$ signal.
R BIT LAST	Receiver Bit Counter Last Count	A2A10P1-20	RCVR 5	RCVR 4 RCVR 20 RCVR 26	HIGH during last bit time of received character.
$\overline{R\ BIT\ LAST}$		A2A10P1-8	RCVR 5	RCVR 4 RCVR 13 RCVR 18	Complement of above.
R CLK-1	Receiver Clock	A2A10P1-32	RCVR 3	RCVR 20 RCVR 4 RCVR 9 RCVR 11	Externally supplied Receiver Clock at twice data rate. Center bit time of received data is at fall of station receiver clock.
$\overline{R\ CLK}$	$\overline{Receiver\ Clock}$	A2A8P1-29	RCVR 2	RCVR 3	Complement of the Station Receiver Clock
$\overline{R\ CLK-1}$	$\overline{Receiver\ Clock-1}$	A2A10P1-30	RCVR 4	RCVR 12	Buffered $\overline{R\ CLK}$
R CLK L	Receiver Clock Line	A2A14TB3-6	Terminal TB3-6	RCVR 2	Station Receiver Clock input line to level converter.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R CLK LR	Receiver Clock Return Line	A2A14TB3-5	Terminal TB3-6	RCVR 2	Return line for above
R CLK ST L	Receiver Clock Step		RCVR 29	Terminal TB5-5	Gated Receiver Clock to data sink once per character in Start/Stop Modes but once per bit in "Bit Stream" mode LOW level DC interface. MIL STD 188C.
$\overline{\text{R CLK ST}}$	Receiver Clock Step	A2A10P1-10	RCVR 9	RCVR 29	Complement of above to drive "Line Driver".
$\overline{\text{R SYNCING}}$	Receiver in "Sync Cycle"	A2A11P1-46	RCVR 25	RCVR 10 XMTR 27	LOW during receiver "synchronizing cycle" Lights sync indicator light and holds system in "ARQ cycle".
$\overline{\text{R IDL DA INH}}$	Received Idle Super Data Inhibit	A2A10P1-29	RCVR 10	RCVR 19	LOW to inhibit receiver data output when idle supervisory character is received.
R IN DA L	Receiver Input Data Line	A2A14TB3-7	Terminal TB3-7	RCVR 1	Receiver input data line to level converter.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R IN DA DL	Receiver Input Data Delayed	---	RCVR 12	RCVR 14 RCVR 13	Receiver input data after being re-timed by station receiver clock.
$\overline{\text{R IN DA DL}}$	Complement of Above	---	RCVR 12	RCVR 13	Complement of above.
R IN DA LR	Receiver Input Data Return Line	A2A14TB3-8	Terminal TB3-7	RCVR 1	Return Line for R IN DA L.
R IN DA-1	Receiver Input Data	A2A10P1-23	RCVR 3	RCVR 12	Receiver input data after level converter and "Test Mode" gates in test mode signal becomes identical to transmitter "SND LIN".
$\overline{\text{R IN DA}}$	$\overline{\text{Receiver Input Data}}$	A2A8P1-56	RCVR 1	RCVR 3	Receiver input data after level-conversion.
$\overline{\text{R N1 CLK}}$	$\overline{\text{Receiver N1 Clock}}$	A2A10P1-48	RCVR 4	RCVR 5 RCVR 6 RCVR 13 RCVR 14 RCVR 21	LOW pulse half fast clock wide (3 micro-sec) after fall of the Receiver Clock.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
R L N2 CLK	Receiver Last N2 Clock	---	RCVR 4	RCVR 22 RCVR 24 RCVR 25 RCVR 27 RCVR 28	HIGH pulse half fast clock wide (3 μsec) one period fast clk (6 μsec) after R CLK during last bit time of received character.
$\overline{\text{R L N2 CLK}}$	$\overline{\text{Receiver Last N2 Clock}}$	A2A10P1-34	RCVR 4	RCVR 7 RCVR 10	Complement of above
$\overline{\text{R IN ARQ}}$	$\overline{\text{Receiver in "ARQ Cycle".}}$	A2A11P1-40	RCVR 24	RCVR 10	LOW during receiver "ARQ Cycle" inhibits received data to data sink terminal and step clock outputs.
R OUT EN	Receiver Output Enable	A2A10P1-28	RCVR 10	RCVR 19	HIGH to enable received data into data terminal (sink) and step clock.
R ARQ FLG	Receiver ARQ Flag	A2A11P1-53	RCVR 26	XMTR 25	HIGH from first character of receiver "ARQ Cycle" to initiate transmitter "ARQ Cycle". Cleared by transmitter on first character of transmitter "ARQ Cycle".

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
$\overline{\text{R RESYNC}}$	$\overline{\text{Receiver Re-synchronized}}$	A2A11P1-26	RCVR 21	RCVR 5 RCVR 28 RCVR 25	LOW pulse at R N1 CLK time if sync supervisory pattern (Sync A followed by Sync B) is received forces receiver bit counter to "Last Bit Time".
$\overline{\text{R SYNC FLG 1}}$	$\overline{\text{Receiver Sync Flag Number One}}$	A2A11P1-22	RCVR 28	XMTR 27	LOW after receiving sync pattern (Sync A followed by Sync B); cleared on last character of transmitter "Sync Cycle".
R SYNC FLG 2	Receiver Sync Flag Number Two	A2A11P1-20	RCVR 28	XMTR 27	LOW after receiving sync pattern followed by correct "Inhibit Activate" or "Inhibit Deactivate" supervisory character check for system synchronization cleared on last character of transmitter "Sync Cycle".
R O DA A	Receiver Output Data A	A2A9P1-35	RCVR 19	RCVR 11	Receiver serial output data from parallel to serial converter and inhibit gate.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
R O DA B	Receiver Output Data B	A2A10P1-25	RCVR 11	RCVR 31	Inverted Receiver Serial output data after being re-timed to station receiver clock.
R O DA L	Receiver Output Data Line	A2A8P1-46	RCVR 31	Terminal TB5-3	Receiver serial output data to terminal (sink) LOW level DC interface. MIL STD 188C.
ST ARQ	Start ARQ Cycle	---	RCVR 26	RCVR 24	Start on ARQ cycle
SUPER RCVD	Supervisory Character Received	A2A10P1-38	RCVR 10	RCVR 16	LOW during last bit time if any supervisory character received except "Idle".
SYNC A RCVD	Sync A Received	A2A9P1-56	RCVR 15	RCVR 10 RCVR 21	LOW during last bit time if Sync A supervisory character being received.
SYNC B RCVD	Sync B Received	A2A9P1-36	RCVR 15	RCVR 10 RCVR 21	LOW during last bit time if Sync B supervisory character being received.
SYNC 0 RCVD	Sync Zeros Received	A2A9P1-50	RCVR 15	RCVR 21	LOW during last bit time if zeros in Sync B supervisory character are received.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
TEST FP	Test Mode Select	A2A12S6-1	Front Panel	RCVR 3	HIGH when front panel "Test Switch" is in test position.
$\overline{\text{TEST FP}}$	$\overline{\text{Test Mode Select}}$	A2A12S6-3	Front Panel	RCVR 3	Complement of above.
TEST IND FP	Test Indicator Front Panel	A2A10P1-22	---	---	Test indicator return path.
$\overline{\text{TEST UNSYNC}}$	$\overline{\text{Test Un-Synchronize}}$	A2A10P1-56	RCVR 7	RCVR 24	LOW pulse after entering Test Mode.
$\overline{\text{UNUSED RCVD}}$	$\overline{\text{Unused Constant Ratio Code Received}}$	A2A9P1-34	RCVR 16	RCVR 20	LOW during last bit time if unused constant ratio code being received
$\overline{\text{X BIT LAST}}$	$\overline{\text{Transmitter Bit Counter Last Count}}$	A2A2P1-11	XMTR 16	RCVR 6	LOW during last count of the transmitter bit counter. Used in receiver to force unsynchronization in test mode.
$\overline{\text{X CLK-1}}$	$\overline{\text{Transmitter Clock-1}}$	A2A3P1-18	XMTR	RCVR 3	Buffered $\overline{\text{X CLK}}$.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER OUTPUT	BLOCK REF. NUMBER INPUT	DESCRIPTION
X CL ARQ FLG	Transmitter Clear ARQ Flag	A2A4P1-4	XMTR 25	RCVR 26	LOW for second two characters of transmitter "ARQ Cycle". Will clear ARQ flag set by receiver.
X CL SYNC FLGS	Transmitter Clear Sync Flags	A2A4P1-10	XMTR 27	RCVR 28	LOW for last character of transmitter "Sync Cycle". Will clear sync flags set by receiver.
X SND LIN	Transmitter Send Line	A2A5P1-14	XMTR 33	RCVR 3	Transmitter serial data output complemented. Used by test mode to form receiver data input.
X SYNCING	Transmitter in "Sync Cycle"	A2A4P1-8	XMTR 27	RCVR 26	LOW during transmitter "Sync Cycle". Inhibits input data and clock step to data source.
5 BIT S-S	5 Bit Start-Stop Mode	A2A12S2-1	Front Panel	RCVR 16	LOW when System Format Switch is in 5 Bit Start-Stop position.
6 BIT S-S	6 Bit Start-Stop Mode	A2A12S2-2	Front Panel	RCVR 18	LOW when System Format Switch is in 6 Bit Start-Stop position.

Table 6-3. (Con't)

MNEMONIC	FULL NAME	ORIGIN	BLOCK REF. NUMBER		DESCRIPTION
			OUTPUT	INPUT	
6 BIT S-S	6 Bit Start-Stop Mode	---	RCVR 18	RCVR 16	Complement of above.
$\overline{\text{7 BIT S-S}}$	$\overline{\text{7 Bit Start-Stop}}$ Mode	A2A12S2-3	Front Panel	RCVR 18	LOW when System Format Switch is in 7 Bit Start-Stop position.
7 BIT S-S	7 Bit Start-Stop Mode	---	RCVR 18	RCVR 16	Complement of above.
$\overline{\text{8 BIT S-S}}$	$\overline{\text{8 Bit Start-Stop}}$ Mode	A2A12S2-4	Front Panel	RCVR 18	LOW when System Format Switch is in 8 Bit Start-Stop position.

Table 6-4. Control Panel Signal Name Glossary

MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
$\overline{\text{ARQ IND FP}}$	$\overline{\text{ARQ Indicator Front Panel}}$	A2A4P1-18	LOW during transmitter "ARQ cycle" to light ARQ front panel indicator.
$\overline{\text{BIT STREAM}}$	$\overline{\text{Bit Stream Format}}$	A2A12S2-5	LOW when format switch on set-up panel is in Bit Stream position.
$\overline{\text{FP INH ACT}}$	$\overline{\text{Front Panel Inhibit Activate}}$	A2A12S5-3	Change from HIGH to LOW causes transmission of Inhibit Activate supervisor.
$\overline{\text{FP INH DEACT}}$	$\overline{\text{Front Panel Inhibit Deactivate}}$	A2A12S5-1	Change from LOW to HIGH causes transmission of Inhibit Deactivate supervisor.
FP SYNC INH	Front Panel "Sync" Inhibit	A2A4P1-35	HIGH when ARQ marker is in active memory address to inhibit from panel sync initiation.
FP SYNC INT	Front Panel "Sync" Initiate	A2A12S3-1	HIGH from sync switch to initiate "sync cycle" when switch is pressed.
$\overline{\text{FP SYNC INT}}$		A2A12S3-3	Complement of above.

Table 6-4. (Con't)

MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
FP TEST	Front Panel Test	A2A12S6-1	HIGH when front panel test switch is in On position.
$\overline{\text{FP TEST}}$		A2A12S6-3	Complement of above.
FP TEST IND RET	Front Panel Test Indicator Return	A2A10P1-22	Return line for "Test" indicator.
$\overline{\text{INH REQ IND FP}}$	$\overline{\text{Inhibit Request Indicator}}$	A2A3P1-5	LOW to light Inhibit Request indicator on front panel when last inhibit supervisory character transmitted was "Inhibit Activate".
$\overline{\text{MC IND FP}}$	$\overline{\text{Mutilated Character Indicator}}$	A2A11P1-S4	LOW to light front panel MC indicator during all but last character of receiver "ARQ Cycle".
MEM LG 4 MEM LG 8 MEM LG 16 MEM LG 32	Memory Length Binary	A2A12S1D-1 A2A12S1D-2 A2A12S1D-4 A2A12S1D-8	MEM LG 4 thru MEM LG 32 are 4-bit bianry output of Memory Length switch on set-up panel which controls length of recirculating memory.
$\overline{\text{PAR FAIL RES}}$	$\overline{\text{Parity Fail Reset}}$	A2A12S4-3	LOW when parity fail reset switch is depressed to reset Parity Fail indicator.

Table 6-4. (Con't)

MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
PAR FAIL IND FP	Parity Fail Indicator	A2A7P1-30	LOW to light front panel "Parity Failure" indicator from time of detected failure until reset.
PWR ON IND	Power On Indicator	A2A2P1-44	LOW to light Power On indicator.
R DIST INH FP	Received Distant Inhibit Activate	A2A3P1-10	LOW to light front panel "Inhibit Received" indicator when distant inhibit activate is received.
SYNC IND FP	"Sync Cycle" Indicator Front Panel	A2A4P1-20	LOW to light front panel "sync cycle" indicator when transmitter or receiver is in "sync cycle".
SMPL ADJ 0	Sample Adjust	A2A12S1C-1	Output (12 binary bits) of center sample adjust switches on set-up panel to allow sampling time to be adjusted in bit stream format. Each increment is one fast clock (6 microsec) delay. Resolution is one sixteenth of one data bit time at 9600 baud.
SMPL ADJ 1		A2A12S1C-2	
SMPL ADJ 2	(12 Binary Bits)	A2A12S1C-4	
SMPL ADJ 3		A2A12S1C-8	
SMPL ADJ 4		A2A12S1B-1	
SMPL ADJ 5		A2A12S1B-2	
SMPL ADJ 6		A2A12S1B-4	
SMPL ADJ 7		A2A12S1B-8	
SMPL ADJ 8		A2A12S1A-1	
SMPL ADJ 9		A2A12S1A-2	
SMPL ADJ 10		A2A12S1A-4	
SMPL ADJ 11		A2A12S1A-8	

Table 6-4. (Con't)

MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
$\overline{\text{5 Bit S-S}}$	$\overline{\text{5 Bit Start-Stop}}$	A2A12S2-1	LOW when format selector switch is in 5 bit S-S position.
$\overline{\text{6 Bit S-S}}$	$\overline{\text{6 Bit Start-Stop}}$	A2A12S2-2	LOW when format selector switch is in 6 bit S-S position.
$\overline{\text{7 Bit S-S}}$	$\overline{\text{7 Bit Start-Stop}}$	A2A12S2-3	LOW when format selector switch is in 7 bit S-S position.
$\overline{\text{8 Bit S-S}}$	$\overline{\text{8 Bit Start-Stop}}$	A2A12S2-4	LOW when format selector switch is in 8 bit S-S position.

Table 6-5. Power Supply Signal Name Glossary

MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
INIT 1	First Initialize Pulse	A2A17PS1 J2-B	HIGH Pulse (50 microsecs) 400 milliseconds after power turn-on or pressing Initialize switch on DC-DC converter.
LOGIC COM	Logic Common	A2A17PS1 J2-F	Common Point and ground for all circuits internal to AN/FYC-12
MEM LG + V	Memory Length Switch Plus Voltage	A2A2P1-43	HIGH to bias memory length switch.
OUT SIG RET	Output Signal Return	A2A17PS1 J2-G	Common Ground return connection for all line driver outputs of AN/FYC-12
$\overline{\text{PWR ON IND}}$	$\overline{\text{Power On Indicator}}$	A2A2P1-44	LOW to light indicator when power is on.
PWR GND	Power Ground	A2A14E1	Chassis Ground connection to AN/FYC-12
PWR NEG GL	Power Negative 6 Volt Line	A1TB1-2	Unswitched negative power input connection.
PWR NEG G SW	Power Negative 6 Volt Switched Line	CB1-1	Negative input connection after circuit breaker switch.

Table 6-5. (Con't)

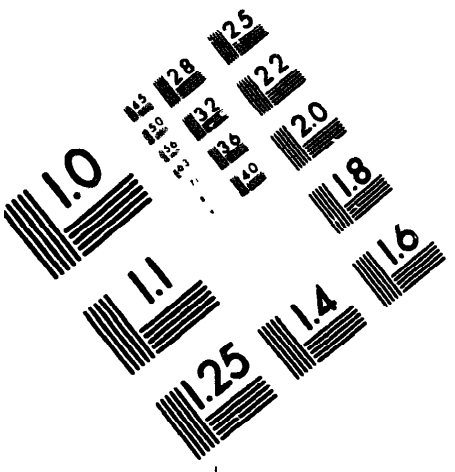
MNEMONIC	FULL NAME	ORIGIN	DESCRIPTION
PWR NEG 12 V	Power Negative 12 Volt Line	A2A17PS1 J2-C	Negative 12 volt output of the DC-DC converter to power line drivers and line receivers.
PWR POS 5 V	Power Positive 5 Volts	A2A17PS1 J2-A	Positive 5 V output of DC-DC converter to power internal logic of AN/FYC-12.
PWR POS GL	Power Positive 6 Volt Line	A1TB1-1	Unswitched positive power input connection.
PWR POS G SW	Power Positive 6 Volt Switched Line	CBI-3	Positive power input after circuit breaker switch.
PWR POS 12V	Power Positive 12 Volts	A2A17PS1	Positive 12 volt output of the DC-DC converter to power "line drivers".
SMPL ADJ + V0 SMPL ADJ + V4 SMPL ADJ + V8	Sample Adjust Switch Plus Voltage	A2A2P1-45 A2A2P1-47 A2A2P1-49	HIGH to bias common terminals of sample adjust switch.
$\overline{5\ BIT\ S\text{-}S}$ $\overline{6\ BIT\ S\text{-}S}$ $\overline{7\ BIT\ S\text{-}S}$ $\overline{8\ BIT\ S\text{-}S}$ $\overline{BIT\ STREAM}$	Format Selector Switch (Plus Voltage)	A2A2P1-51 A2A2P1-53 A2A2P1-55 A2A2P1-57 A2A2P1-40	HIGH to bias common terminals of format adjust switch.

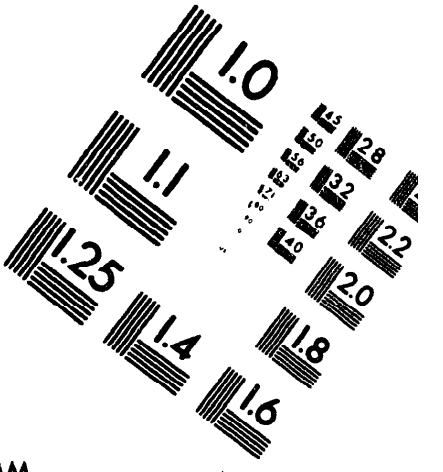
END

9-13-83

DATE

MICROFORM
TEST TARGET





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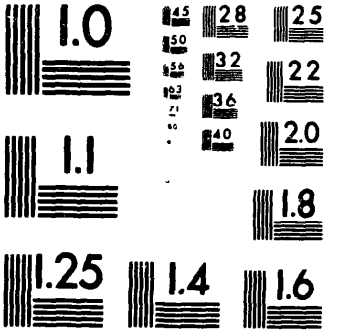

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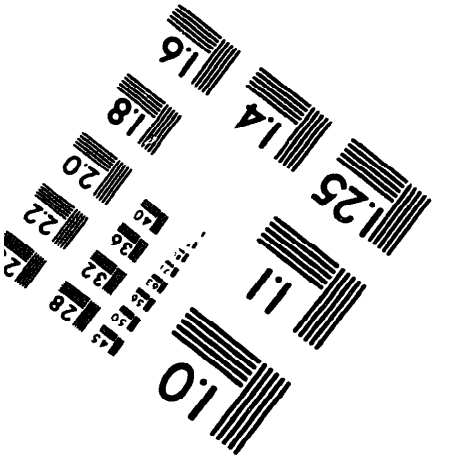

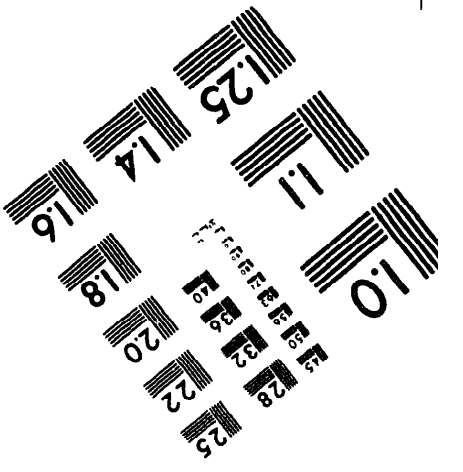

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